

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, M82

MACBOOK AIR (JAN 2007)

PRODUCTION

01/25/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
J		667176	PRODUCTION RELEASED	01/25/09	

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







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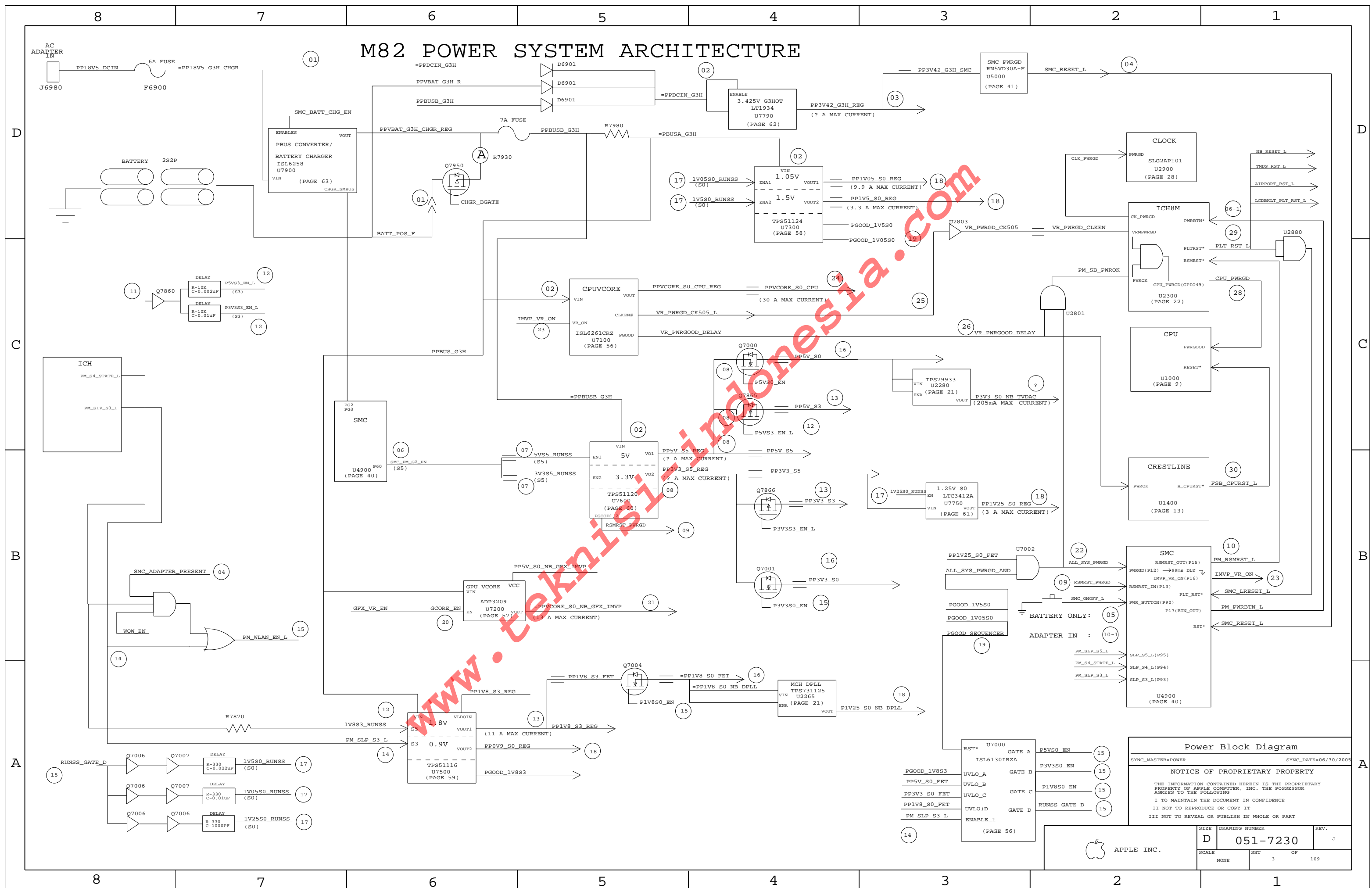
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(MASTER)		73	109	M82 Rule Definitions	(MASTER)	(MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM, MLB, M82	SCH	CRITICAL	
820-2179	1	PCBF, MLB, M82	PCB	CRITICAL	

DRAWING
TITLE=M82_MLB
ABBREV=DRAWING
LAST_MODIFIED=Sun Jan 25 09:33:52 2009

DIMENSIONS ARE IN MILLIMETERS XX ± _____ X.XX ± _____ X.XXX ± _____ ANGLES ± _____ DO NOT SCALE DRAWING	METRIC				 APPLE INC.	
					NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE I I NOT TO REPRODUCE OR COPY IT I I NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
 THIRD ANGLE PROJECTION	DRAFTER		DESIGN CK		TITLE SCHEM, MLB, M82	
	ENG APPD		MFG APPD			
	QA APPD		DESIGNER		DRAWING NUMBER 051-7230	
	RELEASE		SCALE NONE			
	MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	REV. J SPT 1 OF 100		



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826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6																																																																																																																																																																																																										
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7																																																																																																																																																																																																										
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8																																																																																																																																																																																																										
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9																																																																																																																																																																																																										
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA																																																																																																																																																																																																										
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB																																																																																																																																																																																																										
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC																																																																																																																																																																																																										
C	BOMOPTION Groups																																																																																																																																																																																																														
	<table><tr><th>BOM GROUP</th><th colspan="15">BOM OPTIONS</th></tr><tr><td>M82_COMMON</td><td colspan="15">ALTERNATE_COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3</td></tr><tr><td>M82_COMMON1</td><td colspan="15">ISL6258,BOOTROM_FINAL,SMC_PRGRM</td></tr><tr><td>M82_COMMON2</td><td colspan="15">SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB</td></tr><tr><td>M82_COMMON3</td><td colspan="15"></td></tr><tr><td>M82_MICRON</td><td colspan="15">DRAM_MICRON,DRAM_SPD_1</td></tr><tr><td>M82_HYNIX</td><td colspan="15">DRAM_HYNIX,DRAM_SPD_2</td></tr><tr><td>M82_HYNIX_LP</td><td colspan="15">DRAM_HYNIX_LP,DRAM_SPD_2</td></tr><tr><td>M82_SS_CAP</td><td colspan="15">SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF</td></tr><tr><td>M82_MU_CAP</td><td colspan="15">MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF</td></tr><tr><td>M82_TY_CAP</td><td colspan="15">TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF</td></tr></table>																BOM GROUP	BOM OPTIONS															M82_COMMON	ALTERNATE_COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3															M82_COMMON1	ISL6258,BOOTROM_FINAL,SMC_PRGRM															M82_COMMON2	SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB															M82_COMMON3																M82_MICRON	DRAM_MICRON,DRAM_SPD_1															M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2															M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2															M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF															M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF															M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF																													
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	M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2																																																																																																																																																																																																													
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF																																																																																																																																																																																																														
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Module Parts																																																																																																																																																																																																															
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W509S</td><td>U6100</td><td>CRITICAL</td><td>BOOTROM_BLANK_4MB</td></tr><tr><td>341S2111</td><td>1</td><td>IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82</td><td>U6100</td><td>CRITICAL</td><td>BOOTROM_DEVEL</td></tr><tr><td>341S2112</td><td>1</td><td>IC,EFI,BOOTROM_FINAL (LOCKED),M82</td><td>U6100</td><td>CRITICAL</td><td>BOOTROM_FINAL</td></tr><tr><td>337S3477</td><td>1</td><td>SST89V54RD MICROCONTROLLER</td><td>U9300</td><td>CRITICAL</td><td>SST8051_BLANK</td></tr><tr><td>341S2173</td><td>1</td><td>IC,PRGM,SST SST89V54RD,UCN1RLR,M82</td><td>U9300</td><td>CRITICAL</td><td>SST8051_PRGRM</td></tr><tr><td>338S0422</td><td>1</td><td>IC,SMC,HS8/2117</td><td>U4900</td><td>CRITICAL</td><td>SMC_BLANK</td></tr><tr><td>341S2115</td><td>1</td><td>IC,PRGRM,SMC (NEW),M82</td><td>U4900</td><td>CRITICAL</td><td>SMC_PRGRM</td></tr><tr><td>333S0406</td><td>4</td><td>MICRON,DRAM,64M16,8x12.5</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_MICRON</td></tr><tr><td>333S0406</td><td>4</td><td>MICRON,DRAM,64M16,8x12.5</td><td>U3140,U3150,U3160,U3170</td><td>CRITICAL</td><td>DRAM_MICRON</td></tr><tr><td>333S0406</td><td>4</td><td>MICRON,DRAM,64M16,8x12.5</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_MICRON</td></tr><tr><td>333S0406</td><td>4</td><td>MICRON,DRAM,64M16,8x12.5</td><td>U3240,U3250,U3260,U3270</td><td>CRITICAL</td><td>DRAM_MICRON</td></tr><tr><td>333S0411</td><td>4</td><td>HYNIX,DRAM,64M16,8x13</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_HYNIX</td></tr><tr><td>333S0411</td><td>4</td><td>HYNIX,DRAM,64M16,8x13</td><td>U3140,U3150,U3160,U3170</td><td>CRITICAL</td><td>DRAM_HYNIX</td></tr><tr><td>333S0411</td><td>4</td><td>HYNIX,DRAM,64M16,8x13</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_HYNIX</td></tr><tr><td>333S0411</td><td>4</td><td>HYNIX,DRAM,64M16,8x13</td><td>U3240,U3250,U3260,U3270</td><td>CRITICAL</td><td>DRAM_HYNIX</td></tr><tr><td>333S0415</td><td>4</td><td>HYNIX,DRAM,64M16,8x13,LP</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_HYNIX_LP</td></tr><tr><td>333S0415</td><td>4</td><td>HYNIX,DRAM,64M16,8x13,LP</td><td>U3140,U3150,U3160,U3170</td><td>CRITICAL</td><td>DRAM_HYNIX_LP</td></tr><tr><td>333S0415</td><td>4</td><td>HYNIX,DRAM,64M16,8x13,LP</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_HYNIX_LP</td></tr><tr><td>333S0415</td><td>4</td><td>HYNIX,DRAM,64M16,8x13,LP</td><td>U3240,U3250,U3260,U3270</td><td>CRITICAL</td><td>DRAM_HYNIX_LP</td></tr><tr><td>353S1938</td><td>1</td><td>IC,ISL6258,REV2,BAT CHGR, 28P QFN</td><td>U7900</td><td>CRITICAL</td><td>ISL6258</td></tr><tr><td>197S0213</td><td>1</td><td>14.318MHZ XTAL, 2.5x2.0</td><td>Y9390</td><td>CRITICAL</td><td>SST8051_14MHZ</td></tr><tr><td>197S0231</td><td>1</td><td>20MHZ XTAL, 2.5x2.0</td><td>Y9390</td><td>CRITICAL</td><td>SST8051_20MHZ</td></tr><tr><td>197S0257</td><td>1</td><td>33MHZ XTAL, 2.5x2.0</td><td>Y9390</td><td>CRITICAL</td><td>SST8051_33MHZ</td></tr><tr><td>337S3563</td><td>1</td><td>IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU_PRQ_1_6GHZ</td></tr><tr><td>337S3564</td><td>1</td><td>IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU_PRQ_1_8GHZ</td></tr></table>																PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ	337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ	338S0514	1	IC,965GM,CRESTLINE,USFF_BGA	U1400	CRITICAL		338S0515	1	IC,ICH8M,USFF_BGA	U2300	CRITICAL		359S0130	1	LOW POWER CLOCK SYNTHESIZER,SLD3A1811,60PIN	U2900	CRITICAL		335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH, W509S	U6100	CRITICAL	BOOTROM_BLANK_2MB	335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, W509S	U6100	CRITICAL	BOOTROM_BLANK_4MB	341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL	341S2112	1	IC,EFI,BOOTROM_FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL	337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK	341S2173	1	IC,PRGM,SST SST89V54RD,UCN1RLR,M82	U9300	CRITICAL	SST8051_PRGRM	338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK	341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM	333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON	333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON	333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON	333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON	333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX	333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX	333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX	333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX	333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP	333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP	333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP	333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP	353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258	197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ	197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ	197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ	337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ	337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																																																																																																																										
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ																																																																																																																																																																																																										
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ																																																																																																																																																																																																										
338S0514	1	IC,965GM,CRESTLINE,USFF_BGA	U1400	CRITICAL																																																																																																																																																																																																											
338S0515	1	IC,ICH8M,USFF_BGA	U2300	CRITICAL																																																																																																																																																																																																											
359S0130	1	LOW POWER CLOCK SYNTHESIZER,SLD3A1811,60PIN	U2900	CRITICAL																																																																																																																																																																																																											
335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH, W509S	U6100	CRITICAL	BOOTROM_BLANK_2MB																																																																																																																																																																																																										
335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, W509S	U6100	CRITICAL	BOOTROM_BLANK_4MB																																																																																																																																																																																																										
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL																																																																																																																																																																																																										
341S2112	1	IC,EFI,BOOTROM_FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL																																																																																																																																																																																																										
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK																																																																																																																																																																																																										
341S2173	1	IC,PRGM,SST SST89V54RD,UCN1RLR,M82	U9300	CRITICAL	SST8051_PRGRM																																																																																																																																																																																																										
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK																																																																																																																																																																																																										
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM																																																																																																																																																																																																										
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON																																																																																																																																																																																																										
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON																																																																																																																																																																																																										
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON																																																																																																																																																																																																										
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON																																																																																																																																																																																																										
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX																																																																																																																																																																																																										
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX																																																																																																																																																																																																										
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333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP																																																																																																																																																																																																										
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP																																																																																																																																																																																																										
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP																																																																																																																																																																																																										
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP																																																																																																																																																																																																										
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258																																																																																																																																																																																																										
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ																																																																																																																																																																																																										
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ																																																																																																																																																																																																										
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ																																																																																																																																																																																																										
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ																																																																																																																																																																																																										
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ																																																																																																																																																																																																										
B	Alternate Parts																																																																																																																																																																																																														
	<table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>REFERENCE DESIGNATOR(S)</th><th>DESCRIPTION</th><th>BOM OPTION</th></tr><tr><td>128S0093</td><td>128S0092</td><td>ALL</td><td>33UF 20% 16V DCASE</td><td></td></tr><tr><td>376S0466</td><td>376S0410</td><td>ALL</td><td>Si4413 for Si4405</td><td></td></tr><tr><td>740S0044</td><td>740S0028</td><td>ALL</td><td>0.5A OC FUSE</td><td></td></tr><tr><td>104S0023</td><td>104S0018</td><td>ALL</td><td>1206 1/4W .002 OHM</td><td></td></tr><tr><td>152S0684</td><td>152S0421</td><td>ALL</td><td>1.0UH,22A,10MOHM</td><td></td></tr><tr><td>338S0616</td><td>338S0515</td><td>ALL</td><td>USFF PRQ ICH8M B2</td><td></td></tr></table>																PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION	128S0093	128S0092	ALL	33UF 20% 16V DCASE		376S0466	376S0410	ALL	Si4413 for Si4405		740S0044	740S0028	ALL	0.5A OC FUSE		104S0023	104S0018	ALL	1206 1/4W .002 OHM		152S0684	152S0421	ALL	1.0UH,22A,10MOHM		338S0616	338S0515	ALL	USFF PRQ ICH8M B2																																																																																																																																																													
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8	7	6	5	4	3	2	1
ICT Test Points							
These nets have a ICT_TEST property This indicates a MUSTHAVE requirement for ICT							
ICT_TEST							
TRUE PP18V5 DCIN 6 7 50 72	TRUE NB CFG<3> 6 7 13 16	TRUE CK505 PCI5 FCTSEL1 29 30	TRUE DVI HPDET RC 42	TRUE IDE IRQ14 23 38 69	TRUE LVDS A DATA N<2> 7 15 60 67	TRUE P1V8S0 EN 51	TRUE PP18V5 DCIN ONEWIRE 50 72
TRUE BATT POS 6 7 50	TRUE NB CFG<4> 6 7 13 16	TRUE CK505 PCIF0 CLK 29 30	TRUE EXOCARD OC L 24	TRUE IDE PDA<2..0> 23 38 69	TRUE LVDS A DATA P<2> 7 15 60 67	TRUE P3V3S0 EN 51	TRUE PP18V5 G3H 7 8 72
TRUE PP3V3 S5 7 8 72	TRUE NB CFG<5> 6 7 13 16	TRUE CK505 PCIF1 CLK 29 30 71	TRUE EXTAUSB OC F L 39	TRUE IDE PDCS1 L 23 38 69	TRUE LVDS DDC DATA 7 15 60	TRUE P3V3S3 EN L 58	TRUE PP18V5 S5 CHGR SW R 59 72
TRUE PP3V42 G3H 6 7 8 72	TRUE NB CFG<6> 6 7 13 16	TRUE CK505 SRC CLKREQ0 L 7 29 36	TRUE EXTAUSB OC L 9	TRUE IDE PDCS3 L 23 38 69	TRUE LVDS DDC I2C 7 15 60	TRUE P3V3TVDAC EN RC 22	TRUE PP18V5 S5 6 7 8 72
TRUE GND 6 7 13 16	TRUE NB CFG<7> 6 7 13 16	TRUE CK505 USB48 FSA 29 30	TRUE EXTBUSB LVDS EN 9	TRUE IDE PDD<15..0> 23 38 69	TRUE LVDS I2C 7 15 60 67	TRUE P3V3TVDAC NOISE 22	TRUE PP18V5 S5 6 7 8 72
TRUE PM SLP S3 L 6 7 25 36 37	TRUE NB CFG<8> 6 7 13 16	TRUE CK505 XTAL OUT 29	TRUE EXTGPU LVDS EN 7 13 24	TRUE IDE PDDACK L 23 38 69	TRUE LVDS VDD EN 15 60	TRUE P3V42G3H5 BOOST 57	TRUE PP18V5 S5 NB VCCPCE 15 19 21 72
TRUE PM S4 STATE L 6 25 36 41 58	TRUE NB CFG<9> 6 16	TRUE CLINK NB CLK 16 25 70	TRUE EXT COMVID B 43 67	TRUE IDE PDDREQ 23 38 69	TRUE MEM ODT<3..0> 15 23 32	TRUE P3V42G3H SHDN L 57	TRUE PP18V5 S5 6 7 8 72
TRUE PM SLP S5 L 6 25 41 58	TRUE NB RESET L 6 16 28	TRUE CLINK NB DATA 16 25 70	TRUE EXT C R 63 67	TRUE IDE PDIORDY 23 38 69	TRUE MEM RCOMP 16	TRUE P3V42G3H SHDN L1 57	TRUE PP18V5 S5 NB VCCA HPLL 19 21 72
TRUE SMC PM G2 EN 6 16 25	TRUE NB SB SYNC L 6 16 25	TRUE CLINK NB RESET L 16 25 70	TRUE EXT Y G 63 67	TRUE IDE PDIOR L 23 38 69	TRUE MEM RCOMP L 16	TRUE P5VS0 EN 51	TRUE PP18V5 S5 NB VCCD 19 21 72
TRUE INVP VR_ON 6 41 52	TRUE NB TEST1 6 16	TRUE CLK PWRGD 25 29	TRUE FAN RT PWM 7 47	TRUE IDE PDIOM L 23 38 69	TRUE MEM RCOMP VOH 16	TRUE P5VS3 EN L 58	TRUE PP18V5 S5 NB PEGPLL 19 21 72
TRUE GFX VR_EN 6 9 53	TRUE NB TEST2 6 16	TRUE CPU A20M L 6 10 23 66	TRUE FAN RT TACH 7 47	TRUE IDE RESET BUF L 38	TRUE MEM RCOMP VOL 16	TRUE PBUS ISENSE IN NBG 59	TRUE PP18V5 S5 NB PEGPLL_RC 21 72
TRUE SMC BATT CHG EN 6 41 42	TRUE IVO5S0 RUNSS 51 54	TRUE CPU BSEL<0> 10 30 66	TRUE FRANKCARD GPIO 25 43	TRUE IDE RESET L 24 38	TRUE NB ISENSE VR&G 59	TRUE PCIE E R2D C N 36	TRUE PP18V5 S5 NB VCCA DPLLA 19 22 72
TRUE SMC_ONOFF L 6 40 41 42	TRUE IVO5S0 TRIP 54	TRUE CPU BSEL<1> 10 30 66	TRUE FSB CLK CPU N 10 30 71	TRUE IMVP6_BOOT 52	TRUE NB ISENSE SMC 45	TRUE PCIE E R2D C N F 7 36	TRUE PP18V5 S5 NB VCCA DPLLB 19 22 72
TRUE ALL SYS PWRGD AND 6 51	TRUE IVO5S0 RUNSS 51 57	TRUE CPU BSEL<2> 10 30 66	TRUE FSB CLK CPU P 10 30 71	TRUE IMVP6_BOOT RC 52	TRUE NB ISENSE RN L 15	TRUE PCIE E R2D C N F 7 36	TRUE PP18V5 S5 6 7 8 72
TRUE PPVBAT G3H CHGR REG 6 59 72	TRUE IVO5S0 V5FILT 54	TRUE CPU COMP<0> 10 66	TRUE FSB CLK NB N 14 30 71	TRUE IMVP6_COMP R 52	TRUE NB CFG<16> 6 16	TRUE PCIE CLK100M MINI N 36	TRUE PP18V5 S5 NB ODAC 22 72
TRUE CPU PWRGD 6 7 10 13 23 66	TRUE IVO5S0 RUNSS 51 54	TRUE CPU COMP<1> 10 66	TRUE FSB CLK NB P 14 30 71	TRUE IMVP6_DROOP 52	TRUE NB CFG<19> 6 16	TRUE PCIE CLK100M MINI N F 36	TRUE PP18V5 S5 NB VCCD CRT 22 72
TRUE PM RSMRST L 6 25 41	TRUE IVO5S0 TRIP 54	TRUE CPU COMP<2> 10 66	TRUE FSB CPURST L 10 13 14 66	TRUE IMVP6_PHASE 52	TRUE NB CFG<20> 6 16	TRUE PCIE CLK100M MINI P 36	TRUE PP18V5 S5 NB VCCD ODAC 19 22 72
TRUE PM PWRBTN L 6 25 41	TRUE IVO5S3 CS 55	TRUE CPU COMP<3> 10 66	TRUE FWH MFG MODE 25	TRUE IMVP6_PVCC 52	TRUE NB CFG<21> 6 7 13 16	TRUE PCIE CLK100M MINI P F 36	TRUE PP18V5 S5 NB VCCD VDD 22 72
TRUE TP PCI_RST L 9	TRUE IVO5S3 V5FILT 55	TRUE CPU DPRSTP L 6 10 16 23 52	TRUE GCORE BST D 53	TRUE IMVP6_RBIA5 52	TRUE NB CFG<24> 6 7 13 16	TRUE PCIE E D2R N 36	TRUE PP18V5 S5 NB VCCDMPPLL 26 27 72
TRUE PLT_RST L 6 7 24 28	TRUE IVO5S3 VDDOSET 55	TRUE CPU DPRSLP L 6 10 16 23 52	TRUE GCORE_COMP R 53	TRUE IMVP6_SOFT 52	TRUE NB CFG<25> 6 7 13 16	TRUE PCIE E D2R N F 7 36	TRUE PP18V5 S5 NB VCCDMPPLL F 27 72
TRUE SMC RESET L 6 41 42 43	TRUE IVO5S3 CS 56	TRUE CPU FERR L 6 10 23 66	TRUE GCORE_CSEF 53	TRUE IMVP6_VDIFF 52	TRUE NB CFG<26> 6 7 13 16	TRUE PCIE E D2R P 7 36	TRUE PP18V5 S5 NB VCCDMPPLL 26 27 72
TRUE PM_SYSRST L 6 25 28 41	TRUE IVO5S3 TONSEL 56	TRUE CPU GTLREF 10 66	TRUE GCORE_FBRN 53	TRUE IMVP6_VDIFF RC 52	TRUE NB CFG<27> 6 7 13 16	TRUE PCIE E D2R P F 7 36	TRUE PP18V5 S5 6 7 8 72
TRUE PP1V5 S0 6 7 8 72	TRUE IVO5S3 V5FILT 56	TRUE CPU IERR L 10 66	TRUE GCORE_LLNE 53	TRUE IMVP6_VO R 52	TRUE NB CFG<28> 6 7 13 16	TRUE PCIE E R2D C N 36	TRUE PP18V5 S5 ANALOG SDVO F 61 72
TRUE PP1V05 S0 6 7 8 72	TRUE IVO5S3 VREF 56	TRUE CPU IGND L 10 23 66	TRUE GCORE_PMON 53	TRUE IMVP6_VR TT 52	TRUE NB CFG<29> 6 16	TRUE PCIE E R2D C N F 7 36	TRUE PP18V5 S5 ANALOG TMD5 F 61 72
TRUE PP1V8 S0 6 7 8 72	TRUE IVO5S3 VREG3 56	TRUE CPU INIT L 10 23 66	TRUE GCORE_VSEN N 53	TRUE IMVP6_VSEN P 52 66	TRUE NB CLK100M DPLLSS N 9 30	TRUE PCIE E R2D C P F 7 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP1V8 S3 6 7 8 72	TRUE IVO5S3 CS 56	TRUE CPU INTR 10 23 66	TRUE GCORE_PWRGD 53	TRUE IMVP6_VSUM 52	TRUE NB CLK100M DPLLSS P 9 30	TRUE PCIE E R2D N 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP0V9 S0 6 7 8 72	TRUE IVO5S3 VREG 56	TRUE CPU NMI 10 23 66	TRUE GCORE_RAMP 53	TRUE IMVP6_VW 52	TRUE NB CLK100M PCIE N 16 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP0V9 S3 6 7 8 72	TRUE ADAPTER SENSE 50	TRUE CPU PROCHOT BUF 42	TRUE GCORE_RPM 53	TRUE IMVP6_VW 52	TRUE NB CLK100M PCIE P 16 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP1V25 S0 6 7 8 72	TRUE AIRPORT_RST L 7 28 36	TRUE CPU PROCHOT L 42 52 66	TRUE GCORE_RT 53	TRUE IMVP6_DPRSLEVR 52	TRUE NB CLK96M DOT N 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP5V S5 6 7 8 72	TRUE ALL_SYSPWRGD_DLY 51	TRUE CPU PROCHOT L R 42	TRUE GCORE_ST 53	TRUE IMVP6_VR_ON 6 41 52	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP5V S3 6 7 8 72	TRUE ALL_SYS_PWRGD 28 41 51 52	TRUE CPU PWRGD 6 10 13 23 66	TRUE GCORE_SW 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP5V S0 6 7 8 72	TRUE ALL_SYS_PWRGD_AND 6 51	TRUE CPU SMI L 10 23 66	TRUE GCORE_SW R 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP3V3 S3 6 7 8 72	TRUE ARR_DETECT L 25	TRUE CPU STPCLK L 10 23 66	TRUE GCORE_VARFREQ 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP3V3 A S0 6 8	TRUE AUD_MIC_CLK 7 37 60	TRUE CPU THERMD N 10 46 66	TRUE GCORE_VCC 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PP3V3 B S0 6 8	TRUE AUD_MIC_CLK F 60	TRUE CPU THERMD P 10 46 66	TRUE GCORE_VDC DIV 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PPVCORE S0 CPU 6 7 8 72	TRUE AUD_MIC_DATA 7 37 60	TRUE CPU THERMTRIP R 23	TRUE GCORE_VRPM 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PPVCORE S0 NB GFX 6 7 8 72	TRUE AUD_MIC_DATA F 60	TRUE CPU VCCSENSE N 11 52 66	TRUE GCORE_VRPM 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_TCK 6 7 10 13 66	TRUE BATT_POS 6 7 50	TRUE CPU VCCSENSE P 11 52 66	TRUE GFX_VR_EN 6 9 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_TDI 6 7 10 13 66	TRUE BATT_POS F 59	TRUE CPU VID<6..0> 11 52 66	TRUE GLAN_COMP 23 25	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_TDO 6 7 10 13 66	TRUE BOOTROM_OVR_EN L 23 25 43	TRUE CRT_BLUE 63 67	TRUE GND_1V51V05S0_SGND 54	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_TMS 6 7 10 13 66	TRUE CHGR_AGATE 59	TRUE CRT_GREEN 63 67	TRUE GND_1V8S3_SGND 45	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_TRST L 6 7 10 13 66	TRUE CHGR_AMON 59	TRUE CRT_HSYNC_LS 63	TRUE GND_1V8S3_SGND 45	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_CPURST L 6 7 13 66	TRUE CHGR_BOATE 59	TRUE CRT_HSYNC_LS R 63 67	TRUE GND_5V3V3S5_SGND 56	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_BPM_L<4> 6 7 10 13 66	TRUE CHGR_EMON 59	TRUE CRT_HSYNC_R 63 67	TRUE GND_ALS F 60	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_BPM_L<5> 6 7 10 13 66	TRUE CHGR_BOOT 59	TRUE CRT_RED 63 67	TRUE GND_CHGR_SGND 59	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_DBRESET L 6 7 10 13 28	TRUE CHGR_CSIN 59	TRUE CRT_TV0_IREF 63 67	TRUE GND_GCORE_PGND 53	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE XDP_PWRGD 6 7 13	TRUE CHGR_CSIP 59	TRUE CRT_VSYNC_LS 63	TRUE GND_IMVP6_SGND 52	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SPI_A_SCLK R 43 49 69	TRUE CHGR_CSON 59	TRUE CRT_VSYNC_LS R 63	TRUE GND_LCDBKLT_GNDA 64	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SMC_MANUAL_RST L 6 42	TRUE CHGR_CSOP 59	TRUE CRT_VSYNC_R 63 67	TRUE GND_P1V2S3_SGND 64	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SMC_TCK 6 41 42 43	TRUE CHGR_DGIN 59	TRUE DEBUG_RESET L 28 43	TRUE GND_SMC_AVSS 41 42 45 53 59	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SMC_TDI 6 41 42 43	TRUE CHGR_LOWCURRENT_GATE 59	TRUE DLY_OFF_A 51	TRUE HDA_BIT_CLK 9 23 66	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SMC_TDO 6 41 42 43	TRUE CHGR_LOWCURRENT_REF 59	TRUE DLY_OFF_B 51	TRUE HDA_BIT_CLK R 23 66	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SMC_TMS 6 41 42 43	TRUE CHGR_SGATE 59	TRUE DLY_OFF_C 51	TRUE HDA_BIT_CLK R 23 66	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE SMC_TRST L 6 41 43	TRUE CHGR_SGATE_DIV 59	TRUE DLY_OFF_D 51	TRUE HDA_BIT_CLK R 23 66	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE CPU_A20M L 6 10 23 66	TRUE CHGR_VCOMP R 59	TRUE DMI_I2C_COMP R 24	TRUE HDA_RST L 9 23 37 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE CPU_DPRSTP L 6 10 16 23 52	TRUE CHGR_VDD 59	TRUE DMI_N2S_N<3..0> 16 24 67	TRUE HDA_RST L R 9 23 37 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE CPU_DPSLP L 6 10 23 66	TRUE CHGR_VDDP 59	TRUE DMI_N2S_P<3..0> 16 24 67	TRUE HDA_RST L R 9 23 37 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE CPU_FERR L 6 10 23 66	TRUE CHGR_VNEG 59	TRUE DMI_N2N_N<3..0> 16 24 67	TRUE HDA_RST L R 9 23 37 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE NB_BSEL<0> 6 7 13 16 30	TRUE CHGR_VNEG R 59	TRUE DMI_N2N_P<3..0> 16 24 67	TRUE HDA_RST L R 9 23 37 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE NB_BSEL<1> 6 7 13 16 30	TRUE CK505_CLK14P3M_TIMER 38	TRUE DVI_HOST 7 37 63	TRUE HDA_SYNC 9 23 37 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE NB_BSEL<2> 6 7 13 16 30	TRUE CK505_FSA 30 71	TRUE DVI_HOTPLUG_DET 24 61 62	TRUE HDA_SYNC R 23 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE NB_CFG<16> 6 16	TRUE CK505_FSB_TEST_MODE 39	TRUE DVI_HOTPLUG_DET_BUF 61 62	TRUE HDA_SYNC R 23 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE NB_CFG<19> 6 16	TRUE CK505_FSC 30 71	TRUE DVI_HOTPLUG_DET_DEL L 62	TRUE HDA_SYNC R 23 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE NB_CFG<20> 6 16	TRUE CK505_PC13_CLK 29 30 71	TRUE DVI_HOTPLUG_DET_INT L 62	TRUE HDA_SYNC R 23 69	TRUE INT_PIRQA L 24 70	TRUE NB CLK96M DOT P 9 30 71	TRUE PCIE E R2D P 36	TRUE PP18V5 S5 NB VCCD TMD5 F 61 72
TRUE PPVBAT G3H CHGR OUT 59 72	TRUE SB_INTVRMEN 23	TRUE SMC_BS_ALRT L 7 41 42 50	TRUE SMC_TMS L 42	TRUE TMD5_TX_CLK N 52	TRUE VGA_B 57	TRUE PM_RSMRST L 6 25 41	TRUE PP5V S0 6 7 8 72
TRUE PPVBAT G3H CHGR REG 6 59 72	TRUE SB_LAN100_SLP 23	TRUE SMC_CASE_OPEN 41 42	TRUE SMC_TRST L 42	TRUE TMD5_TX_CLK P 52 62	TRUE VGA_G 57	TRUE PM_S4_STATE L 25 41	TRUE PP5V S0 DVIPORT 6 7 8 72
TRUE PPVBAT G3H CHGR REG_O 59 72	TRUE SB_RCIN L 23	TRUE SMC_DCIN_ISENSE 41 59	TRUE SMC_TX L 42	TRUE TMD5_TX_CONN_CLK N 52	TRUE VGA_HSYN 57	TRUE PM_SB_PWRK 25 41	TRUE PP5V S0 DVIPORT D 63 72
TRUE PPVBAT G3H CHGR REG_R 59 72	TRUE SB_RTC_RST L 23 28	TRUE SMC_EXTAL 41 42	TRUE SMC_VCL 42	TRUE TMD5_TX_CONN_CLK P 52	TRUE VGA_R 57	TRUE PM_SLP S3 L 25 41	TRUE PP5V S0 IMVP6_VDD 52 72
TRUE PPVCORE S0 CPU 6 7 8 72	TRUE SB_RTC_X1 23 28	TRUE SMC_FAN_O_CTL 41 47	TRUE SMC_WAKE SCI L 42	TRUE TMD5_TX_CONN_N<2..0> 52	TRUE VGA_VSYN 57	TRUE PM_SLP S4 L85V 25 41	TRUE PP5V S0 KBDLED F 7 40 72
TRUE PPVCORE S0 NB GFX 6 7 8 72	TRUE SB_RTC_X1 R 23 28	TRUE SMC_XTAL 41 47	TRUE SMC_XTAL 42	TRUE TMD5_TX_CONN_P<2..0> 52	TRUE VR_PWRGD CK505 57	TRUE PM_SLP S5 L 25 41	TRUE PP5V S0 S5 VREF 26 27 72
TRUE PPVDCIN G3H PRE 45 72	TRUE SB_RTC_X2 23 28	TRUE SMC_GPU_ISENSE 41 53	TRUE SMS_MONI_EN 42	TRUE TMD5_TX_N<2..0> 52	TRUE VR_PWRGD CK505 57	TRUE PM_STPCPU L 25 30	TRUE PP5V S0 TMD5 FUSE 63 72
TRUE PPVDCIN G3H PRE2 59 72	TRUE SB_SLOAD 25	TRUE SMC_GPU_VSENSE 41 45	TRUE SMS_ONOFF L 42	TRUE TMD5_TX_P<2..0> 52	TRUE VR_PWRGD CK505 57	TRUE PM_STPCCI L 25 30	TRUE PP5V S3 6 7 8 72
TRUE PPVDCIN G3H PRE_O 59 72	TRUE SB_SM_INTRUDER L 23 28	TRUE SMC_KBC_MDE 41 45	TRUE SMS_X_AXIS 42	TRUE TV_A_DAC 46	TRUE WOL_EN 24	TRUE PM_SUS_STAT L 25 41	TRUE PP5V S3 CAMERA_F 7 40 72
TRUE PPVDCIN G3H PRE_R 59 72	TRUE SB_SPKR 25	TRUE SMC_LID 41 45	TRUE SMS_Y_AXIS 42	TRUE TV_B_DAC 46	TRUE WOL_EN 24	TRUE PM_SYSRST L 6 25 28 41	TRUE PP5V S3 TOPCASE_F 7 40
TRUE PPVIN S5 IMVP6 VIN 52 72	TRUE SDVO_CTRLCLK 16 61	TRUE SMC_LRESET L 41 45	TRUE SMS_Z_AXIS 42	TRUE TV_C_DAC 46	TRUE XDP_BPM L<0> 15 23	TRUE PM_THRMTRIP L 15 23	TRUE PP5V S3 USB2_EXT_A 39 72
TRUE PPVOUIT S0 LCDBKLT 7 60 64 72	TRUE SDVO_CTRLDATA 16 61	TRUE SMC_MANUAL_RST L 41 45	TRUE SPI_A_INT_CLK 49	TRUE TV_DCONSEL<1> 46	TRUE XDP_BPM L<1> 15 23	TRUE PM_THRM L 25	TRUE PP5V S3 USB2_EXT_A F 7 37 39 72
TRUE PPVOUIT S0 LCDBKLT SW 64 72	TRUE SMBUS_SB_ME_SCL 44	TRUE SMC_MANUAL_RST L 41 45	TRUE SPI_A_INT_HOLD L 49	TRUE TV_DCONSEL<1> 46	TRUE XDP_BPM L<2> 15 23	TRUE PM_WLAN_EN L 36	TRUE PP5V S5 6 7 8 72
TRUE RSMRST_PWRGD 41 42 56	TRUE SMBUS_SB_ME_SDA 44	TRUE SMC_MDI 41 43	TRUE SPI_A_INT_SI 49	TRUE TV_DCONSEL<1> 46			

FUNC TEST - BATTERY CONNECTOR			FUNC TEST - XDP/ITP CONNECTOR			FUNC TEST - Power Supplies						
x3	R44	TRUE	BATT_POS	6	50	R92	PPVCORE_S0_CPU	6	8	72		
x3	R45	TRUE	GND	6	41	R93	PP0V9_S0	6	8	72		
	R46	TRUE	SMC_BS_ALRT_L	6	41	R94	PP1V05_S0	6	8	72		
	R47	TRUE	SMBUS_SMC_BSA_SCL	6	44	R95	PP1V25_S0	6	8	72		
	R98	TRUE	SMBUS_SMC_BSA_SDA	6	44	R96	PP1V5_S0	6	8	72		
FUNC TEST - DC-IN CONNECTOR			FUNC TEST - TEMP SENSOR CONNECTOR			FUNC TEST - M93 WIRELESS CONNECTOR						
x2	R48	TRUE	PP18V5_DCIN	6	50	72	PP5V_S0	6	8	72		
	R99	TRUE	SYS_ONEWIRE	6	41	R100	PP3V3_S0	6	8	72		
x2	R70	TRUE	GND	6	41	R101	PP1V8_S3	6	8	72		
	R99	TRUE	SMBUS_SMC_0_S0_SCL	6	44	R102	PP3V3_S3	6	8	72		
	R99	TRUE	SMBUS_SMC_0_S0_SDA	6	44	R103	PP5V_S3	6	8	72		
	R99	TRUE	=PP3V3_S0_THRM_SNR	8	46	R104	PP3V3_S5	6	8	72		
FUNC TEST - FAN CONNECTOR			FUNC TEST - CAMERA USB, LVDS, ALS			FUNC TEST - M93 WIRELESS CONNECTOR						
	R65	TRUE	=PP5V_S0_FAN	8	47	R105	PLT_RST_L	6	24	28		
	R66	TRUE	FAN_RT_PWM	6	47	R106	PCIE_WAKE_L	6	7	28	36	
	R66	TRUE	FAN_RT_TACH	6	47	R107	CK505_SRC_CLKREQ6_L	6	7	28	36	
	R68	TRUE	GND	6	47	R108	PCIE_CLK100M_MINI_N_F	6	36			
	R68	TRUE	GND	6	47	R109	PCIE_CLK100M_MINI_P_F	6	36			
x2	R69	TRUE	PP5V_S3_CAMERA_F	6	40	72	PCIE_E_D2R_N_F	6	36			
	R70	TRUE	USB2_CAMERA_F_P	6	40	69	PCIE_E_D2R_P_F	6	36			
	R71	TRUE	USB2_CAMERA_F_N	6	40	69	PCIE_E_R2D_C_N_F	6	7	36		
	R72	TRUE	LCDCLKLT_RTIN<1..6>	6	40	64	PCIE_E_R2D_C_P_F	6	7	36		
	R73	TRUE	LVDS_A_DATA_N<0..2>	6	15	60	67	AIRPORT_RST_L	6	7	28	36
	R74	TRUE	LVDS_A_DATA_P<0..2>	6	15	60	67	SMB_AIRPORT_CONN_CLK	6	36		
	R75	TRUE	PPVOIT_S0_LCDCLKLT	6	40	64	72	SMB_AIRPORT_CONN_DATA	6	36		
	R76	TRUE	LVDS_A_CLK_F_N	6	40			PCIE_E_R2D_C_N_F	6	7	36	
	R77	TRUE	LVDS_A_CLK_F_P	6	40			PCIE_E_R2D_C_P_F	6	7	36	
	R78	TRUE	LVDS_DDC_CLK	6	15	60						
	R79	TRUE	LVDS_DDC_DATA	6	15	60						
	R80	TRUE	PP3V3_S0_LCD_F	6	40	72						
x2	R81	TRUE	PP3V3_LCDVDD_SW_F	6	40	72						
	R82	TRUE	=I2C_TOP_ALS_SDA	44	60							
	R83	TRUE	=I2C_TOP_ALS_SCL	44	60							
x1	R84	TRUE	GND	44	60							
FUNC TEST - AUDIO CONNECTOR			FUNC TEST - RIO HATCH CONNECTOR			FUNC TEST - M93 WIRELESS CONNECTOR						
	R44	TRUE	HDA_SYNC	6	9	23	37	69	PP3V3_S3_AP_AUX	6	36	72
	R45	TRUE	HDA_BITCLK	9	37							
	R46	TRUE	AUD_MIC_DATA	6	37	60						
	R47	TRUE	HDA_SDATAOUT	9	37							
	R48	TRUE	=PPVIN_S0_AUDIO	9	37							
	R49	TRUE	HDA_SDATAIN0	9	37							
	R50	TRUE	AUD_MIC_CLK	6	37	60						
	R51	TRUE	PM_SLP_S3_L	6	25	36	41					
FUNC TEST - IPD CONNECTOR			FUNC TEST - AIRPORT			FUNC TEST - M93 WIRELESS CONNECTOR						
	R52	TRUE	SMC_LID	6	40	41					</	

TR00	TRUE	TP LVDS VBG	==	NC LVDS VBG	
TR01	TRUE	TP NB_RSVD<31>	==	MAKER_BASE+TRUE NC NB_RSVD 31	
TR02	TRUE	TP NB_RSVD<32>	==	MAKER_BASE+TRUE NC NB_RSVD 32	
TR03	TRUE	TP NB_RSVD<33>	==	MAKER_BASE+TRUE NC NB_RSVD 33	
TR04	TRUE	TP MEM_A RCVEN 1	==	MAKER_BASE+TRUE NC MEM_A RCVEN 1	
TR05	TRUE	TP MEM_B RCVEN 1	==	MAKER_BASE+TRUE NC MEM_B RCVEN 1	
TR06	TRUE	TP NB_RSVD<1>	==	MAKER_BASE+TRUE NC NB_RSVD 1	
TR07	TRUE	TP NB_RSVD<2>	==	MAKER_BASE+TRUE NC NB_RSVD 2	
TR08	TRUE	TP NB_RSVD<3>	==	MAKER_BASE+TRUE NC NB_RSVD 3	
TR09	TRUE	TP NB_RSVD<4>	==	MAKER_BASE+TRUE NC NB_RSVD 4	
TR10	TRUE	TP NB_RSVD<5>	==	MAKER_BASE+TRUE NC NB_RSVD 5	
TR11	TRUE	TP NB_RSVD<6>	==	MAKER_BASE+TRUE NC NB_RSVD 6	
TR12	TRUE	TP NB_RSVD<7>	==	MAKER_BASE+TRUE NC NB_RSVD 7	
TR13	TRUE	TP NB_RSVD<8>	==	MAKER_BASE+TRUE NC NB_RSVD 8	
TR14	TRUE	TP NB_RSVD<14>	==	MAKER_BASE+TRUE NC NB_RSVD 14	
TR15	TRUE	TP NB_RSVD<21>	==	MAKER_BASE+TRUE NC NB_RSVD 21	
TR16	TRUE	TP NB_RSVD<22>	==	MAKER_BASE+TRUE NC NB_RSVD 22	
TR17	TRUE	TP NB_RSVD<23>	==	MAKER_BASE+TRUE NC NB_RSVD 23	
TR18	TRUE	TP NB_RSVD<24>	==	MAKER_BASE+TRUE NC NB_RSVD 24	
TR19	TRUE	TP NB_RSVD<25>	==	MAKER_BASE+TRUE NC NB_RSVD 25	
TR20	TRUE	TP NB_RSVD<26>	==	MAKER_BASE+TRUE NC NB_RSVD 26	
TR21	TRUE	TP NB_RSVD<27>	==	MAKER_BASE+TRUE NC NB_RSVD 27	
TR22	TRUE	TP NB_RSVD<35>	==	MAKER_BASE+TRUE NC NB_RSVD 35	
TR23	TRUE	TP NB_RSVD<36>	==	MAKER_BASE+TRUE NC NB_RSVD 36	
TR24	TRUE	TP NB_CFG<10>	==	MAKER_BASE+TRUE NC NB_CFG 10	
TR25	TRUE	TP NB_CFG<11>	==	MAKER_BASE+TRUE NC NB_CFG 11	
TR26	TRUE	TP NB_CFG<14>	==	MAKER_BASE+TRUE NC NB_CFG 14	
TR27	TRUE	TP NB_CFG<15>	==	MAKER_BASE+TRUE NC NB_CFG 15	
TR28	TRUE	TP NB_CFG<17>	==	MAKER_BASE+TRUE NC NB_CFG 17	
TR29	TRUE	TP NB_NC<1>	==	MAKER_BASE+TRUE NC NB_NC 1	
TR30	TRUE	TP NB_NC<2>	==	MAKER_BASE+TRUE NC NB_NC 2	
TR31	TRUE	TP NB_NC<3>	==	MAKER_BASE+TRUE NC NB_NC 3	
TR32	TRUE	TP NB_NC<4>	==	MAKER_BASE+TRUE NC NB_NC 4	
TR33	TRUE	TP NB_NC<5>	==	MAKER_BASE+TRUE NC NB_NC 5	
TR34	TRUE	TP NB_NC<6>	==	MAKER_BASE+TRUE NC NB_NC 6	
TR35	TRUE	TP NB_NC<7>	==	MAKER_BASE+TRUE NC NB_NC 7	
TR36	TRUE	TP NB_NC<8>	==	MAKER_BASE+TRUE NC NB_NC 8	
TR37	TRUE	TP NB_NC<9>	==	MAKER_BASE+TRUE NC NB_NC 9	
TR38	TRUE	TP NB_NC<10>	==	MAKER_BASE+TRUE NC NB_NC 10	
TR39	TRUE	TP NB_NC<11>	==	MAKER_BASE+TRUE NC NB_NC 11	
TR40	TRUE	TP NB_NC<12>	==	MAKER_BASE+TRUE NC NB_NC 12	
TR41	TRUE	TP NB_NC<13>	==	MAKER_BASE+TRUE NC NB_NC 13	
TR42	TRUE	TP NB_NC<14>	==	MAKER_BASE+TRUE NC NB_NC 14	
TR43	TRUE	TP NB_RSVD<29>	==	MAKER_BASE+TRUE NC NB_RSVD 29	
TR44	TRUE	TP NB_RSVD<28>	==	MAKER_BASE+TRUE NC NB_RSVD 28	
TR45	TRUE	TP NB_RSVD<30>	==	MAKER_BASE+TRUE NC NB_RSVD 30	
TR46	TRUE	CRT_DDC_CLK	==	MAKER_BASE+TRUE NC CRT_DDC_CLK	
TR47	TRUE	CRT_DDC_DATA	==	MAKER_BASE+TRUE NC CRT_DDC_DATA	

NO_TEST

NO_TEST

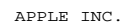
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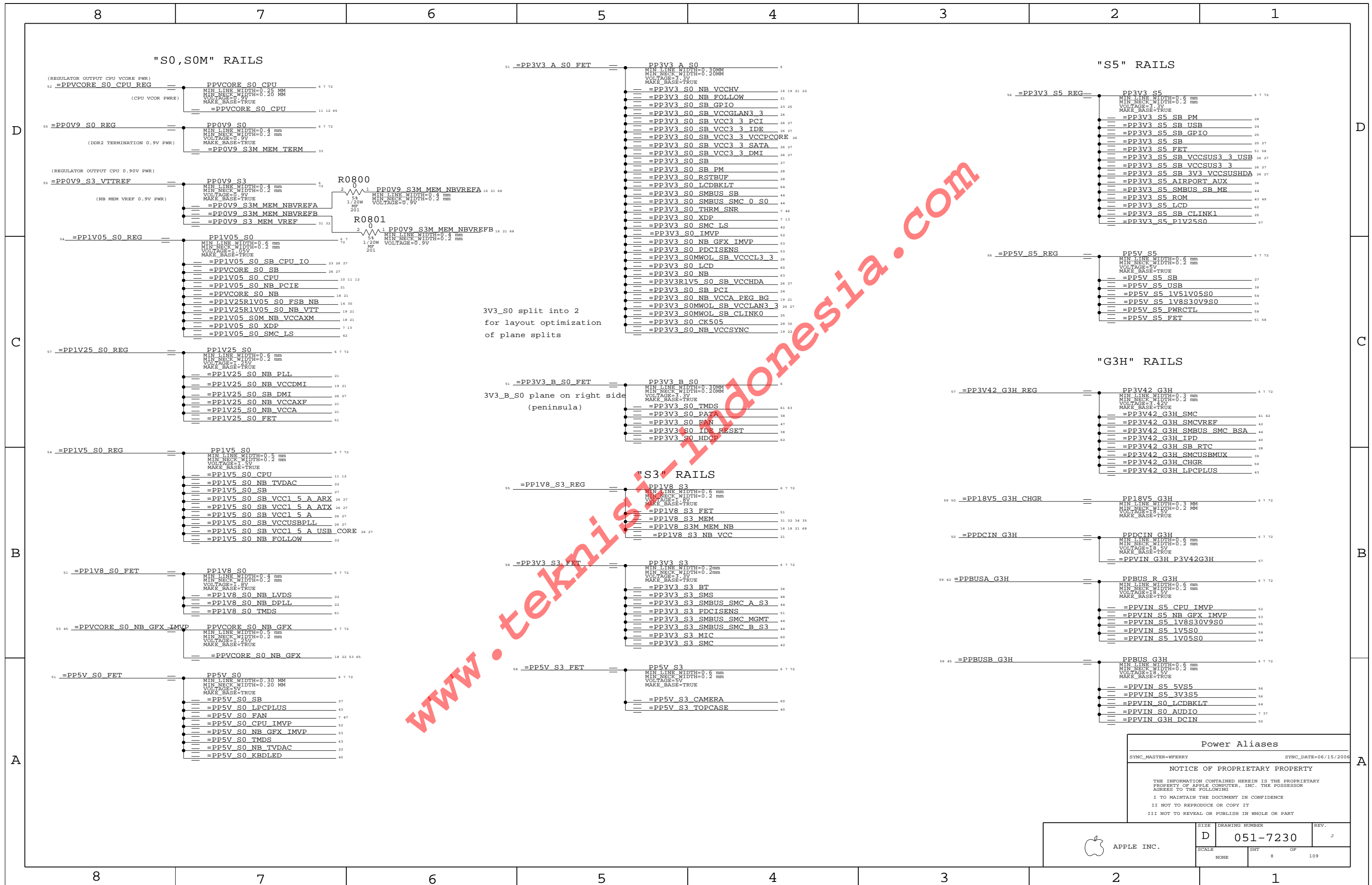
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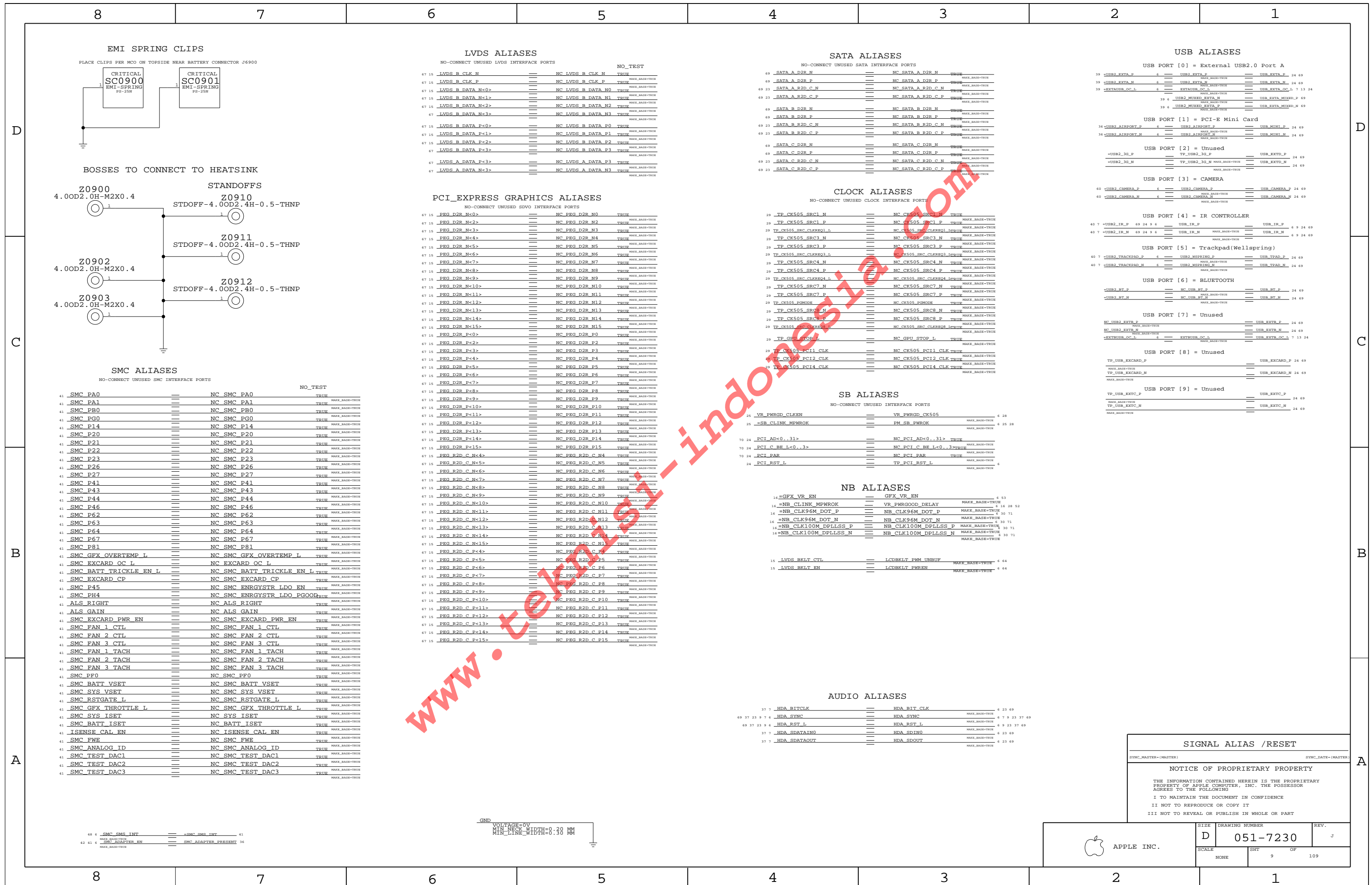
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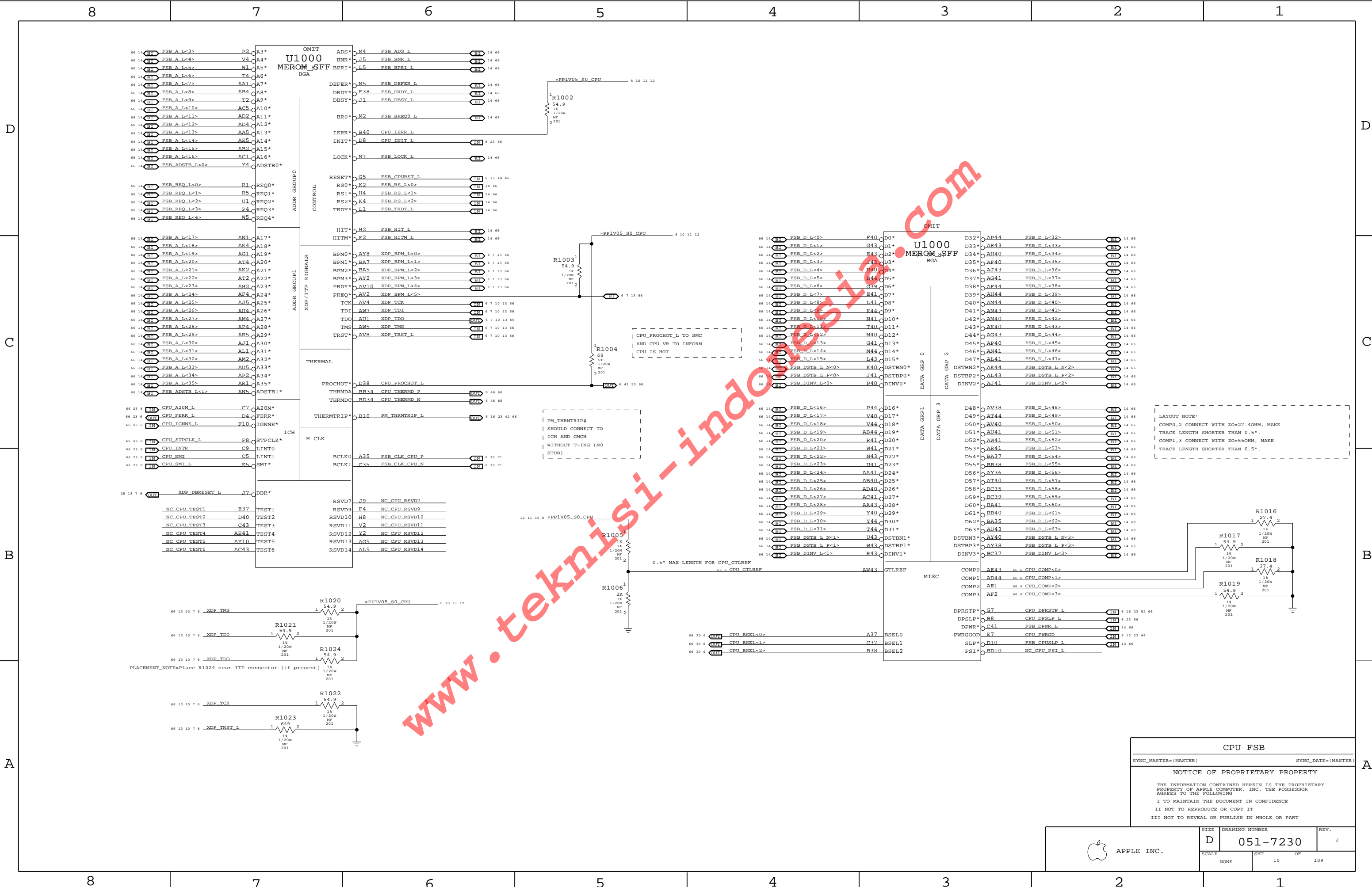
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SIZE D	DRAWING NUMBER 051-7230	REV. J
SCALE NONE	SHT 7	OF 109







CPU FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

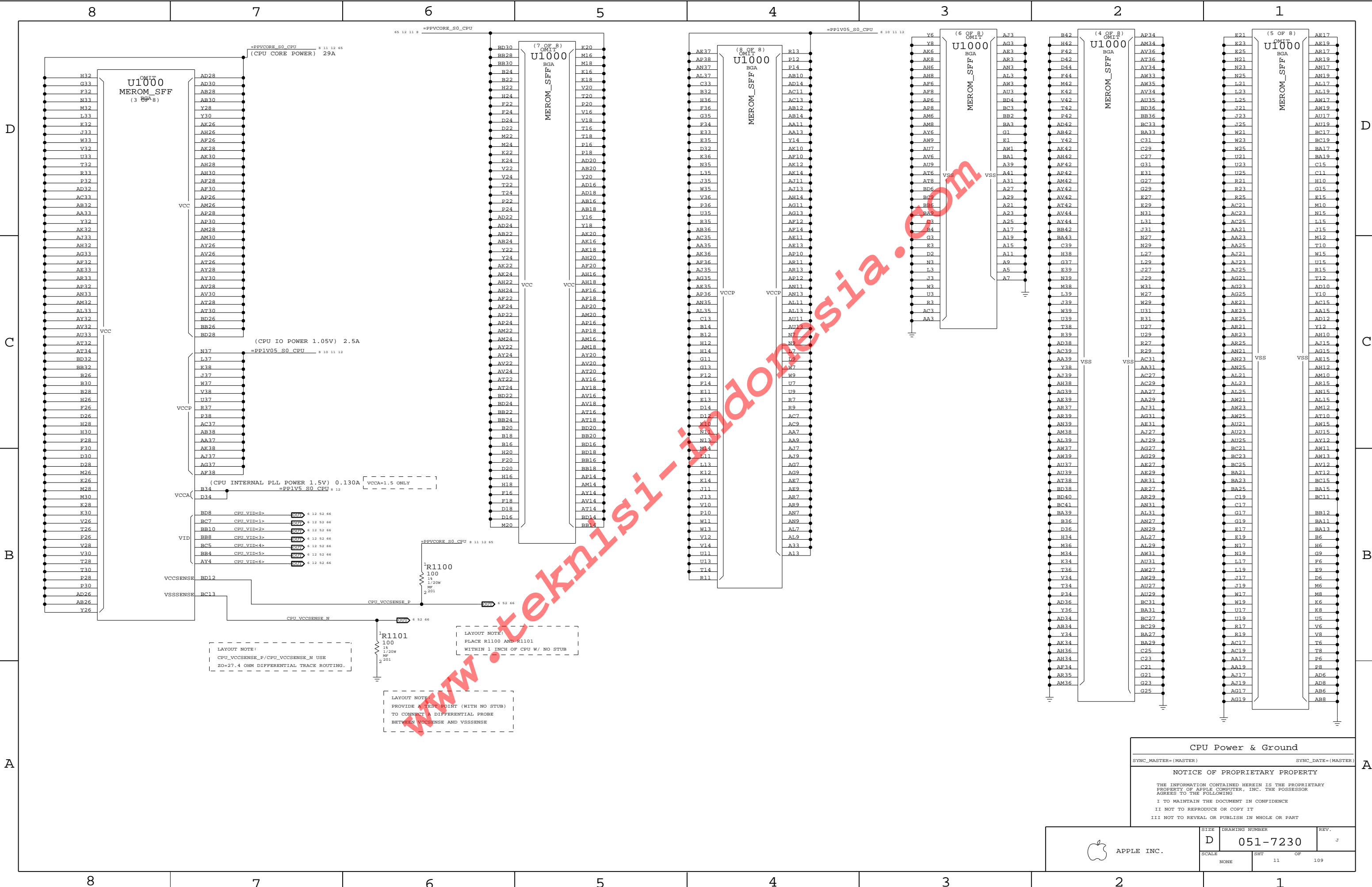
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CPU Power & Ground

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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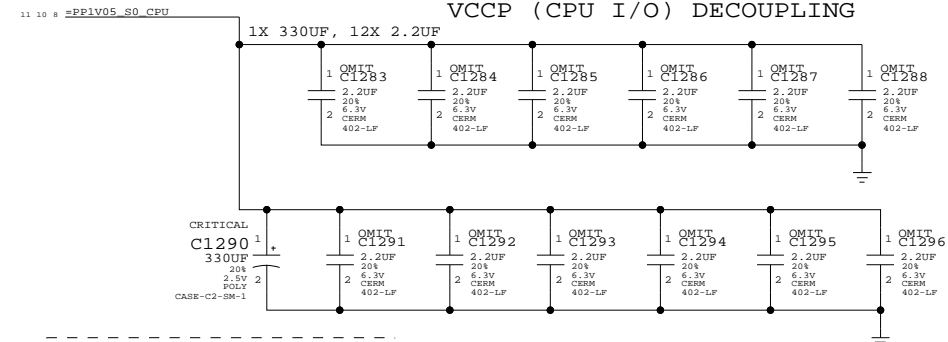
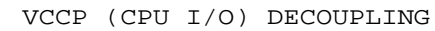
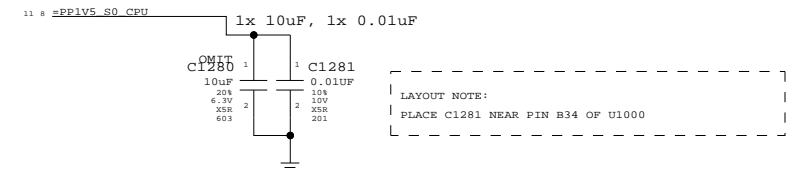
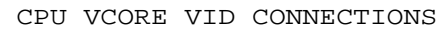
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
SCALE		SHT	OF
NONE		11	109

3x 330uF. 32x 10uF 0603, 28x 1uF 0402
Intel recommends 32+28 but is evaluating 24+24



```

| LAYOUT NOTE:
| PLACE C1290 CLOSE TO CPU
| PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
| PLACE C1291-C1296 CLOSE TO FSB DATA PINS

```

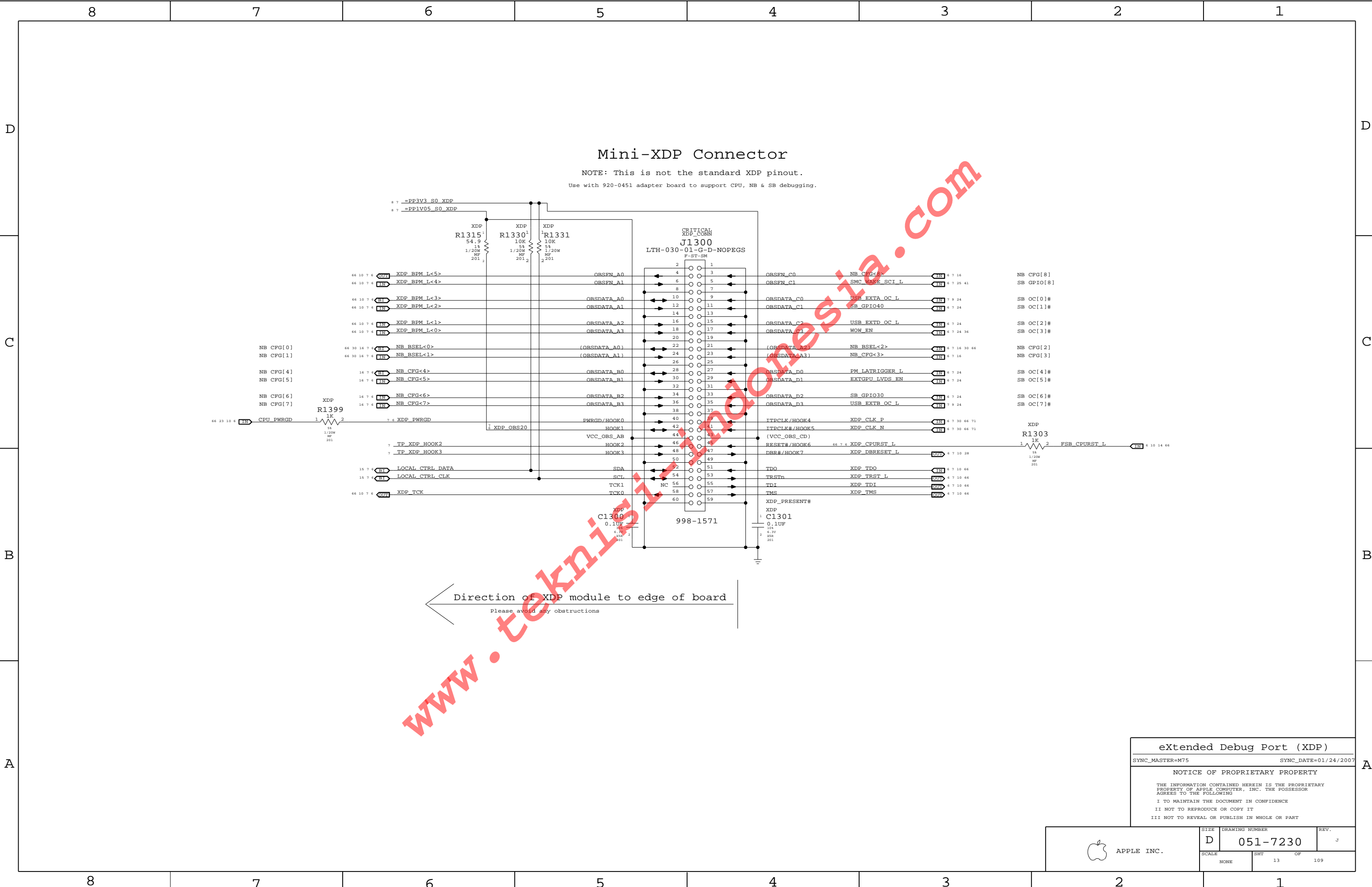
CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006


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eXtended Debug Port (XDP)			
SYNC_MASTER=M75		SYNC_DATE=01/24/2007	
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SCALE	NONE	SHT	13 OF 109



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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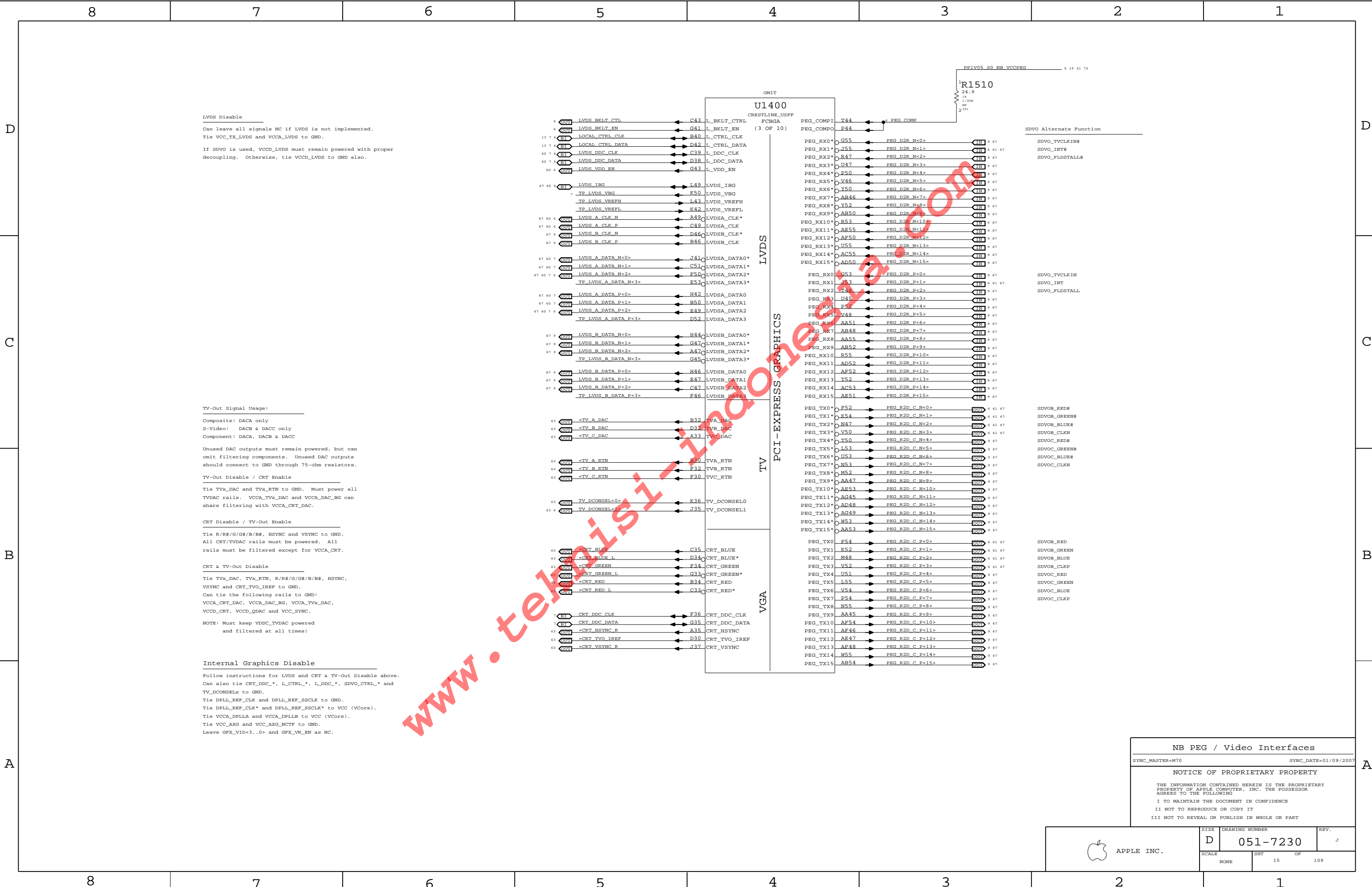
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NONE		14	109	



LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACA & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TV0_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLL and VCCA_DPLL to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.

NB PEG / Video Interfaces

SYNC_MASTER=M70

SYNC_DATE=01/09/2007

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APPLE INC.

SCALE
NONE

SIZE
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DRAWING NUMBER
051-7230

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NB DDR2 Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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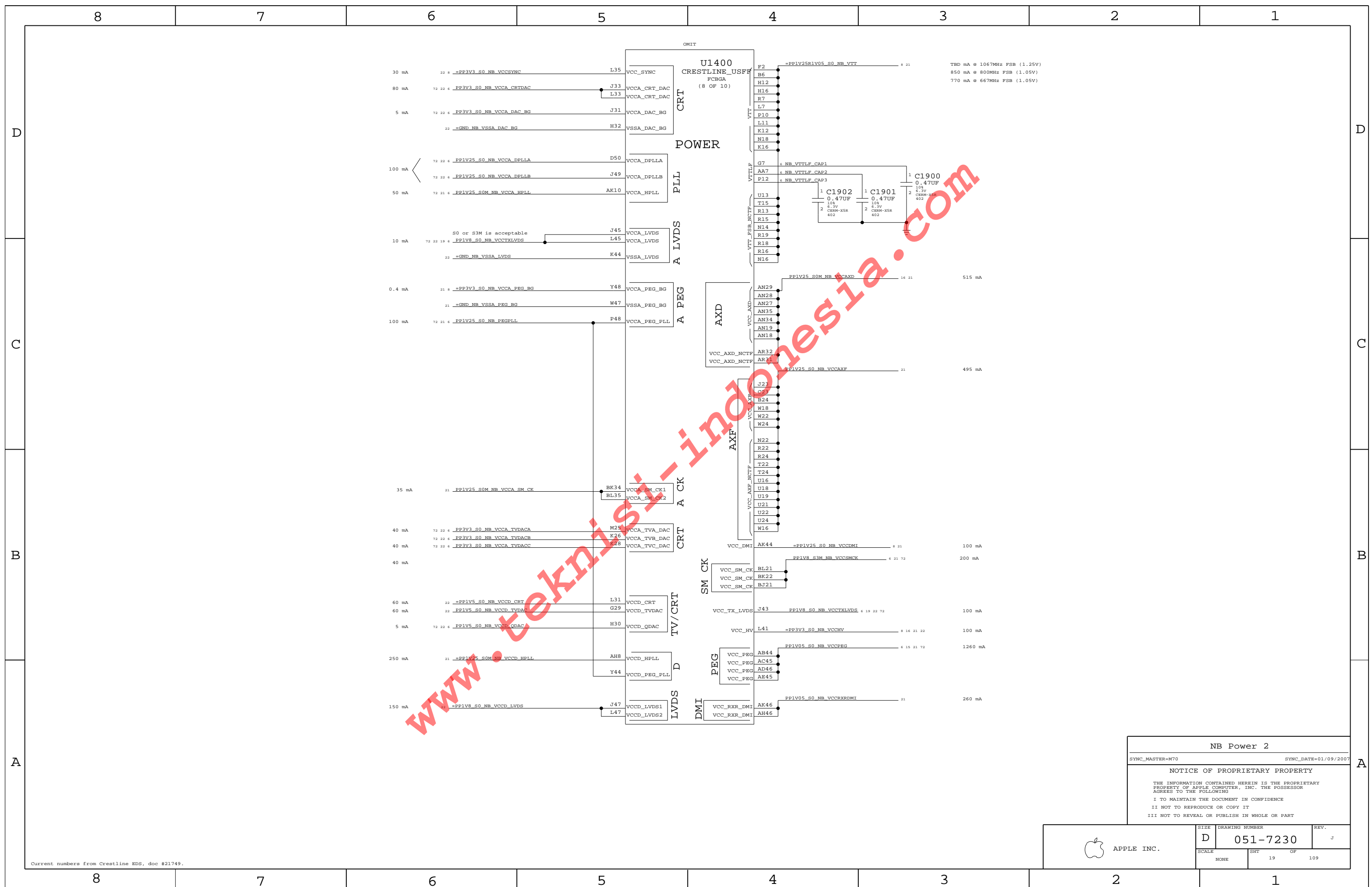
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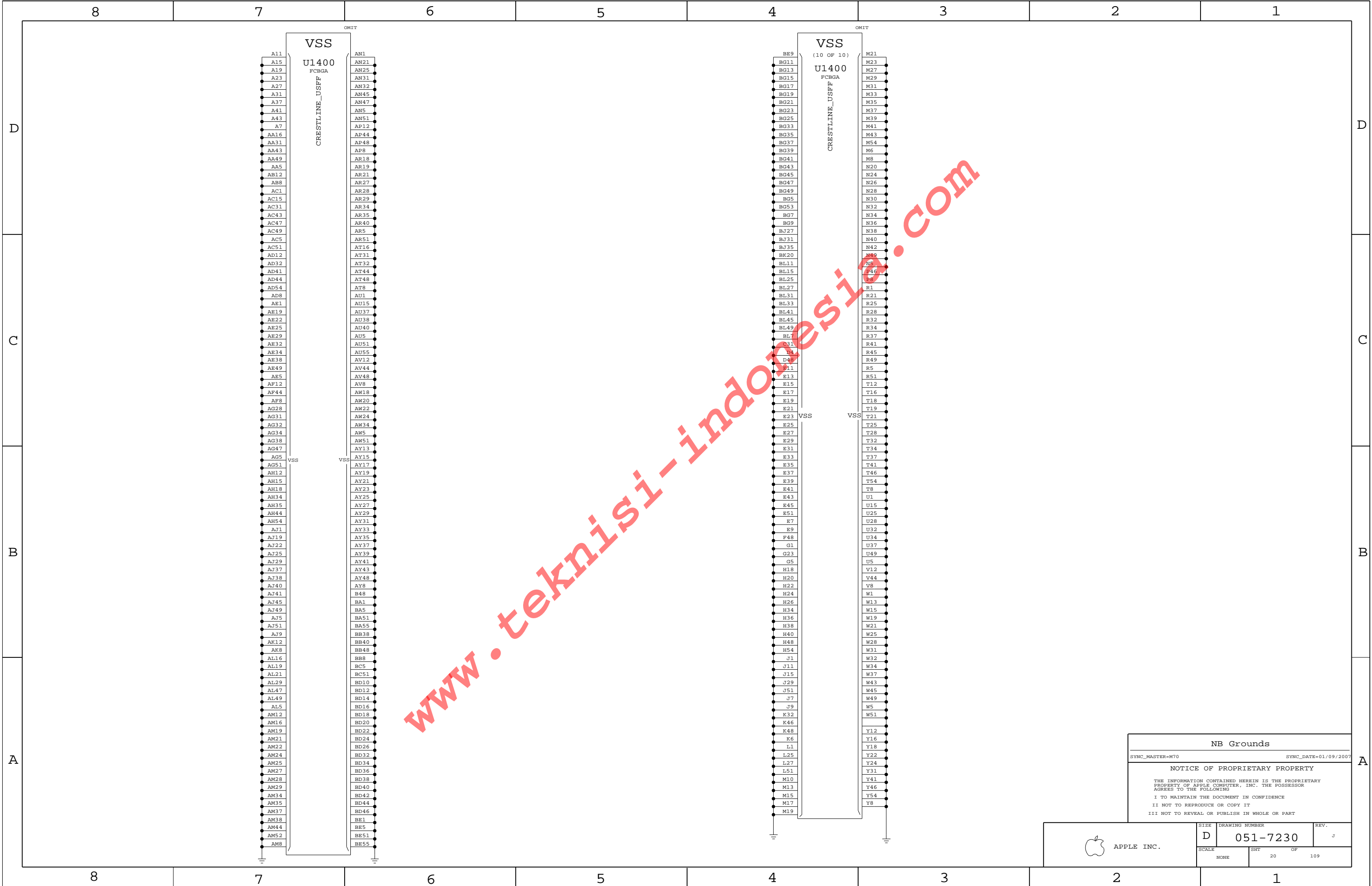
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SCALE		NONE	SHT 17 OF 109	





NB Grounds

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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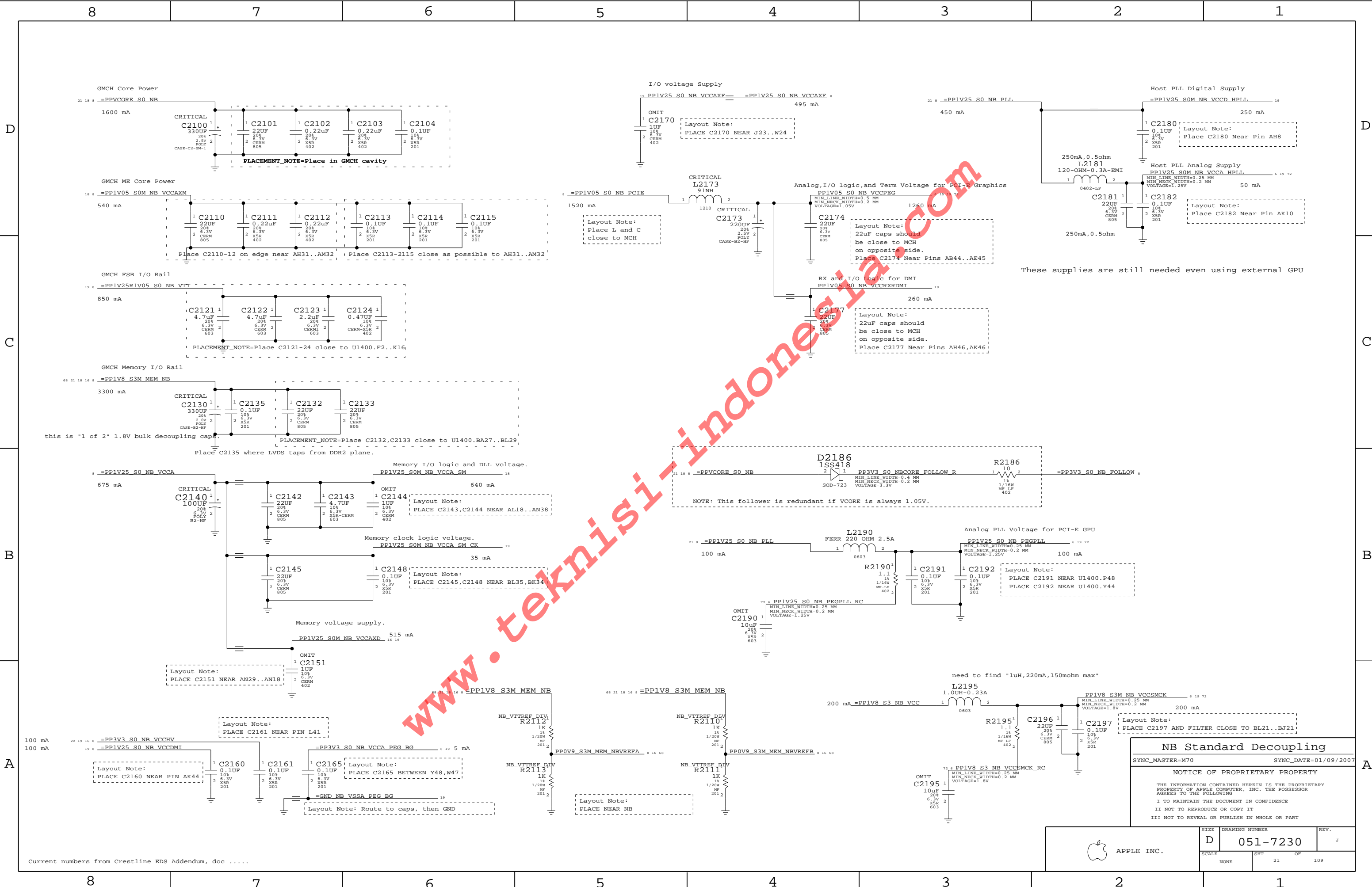
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SCALE		SHT	OF	REV.
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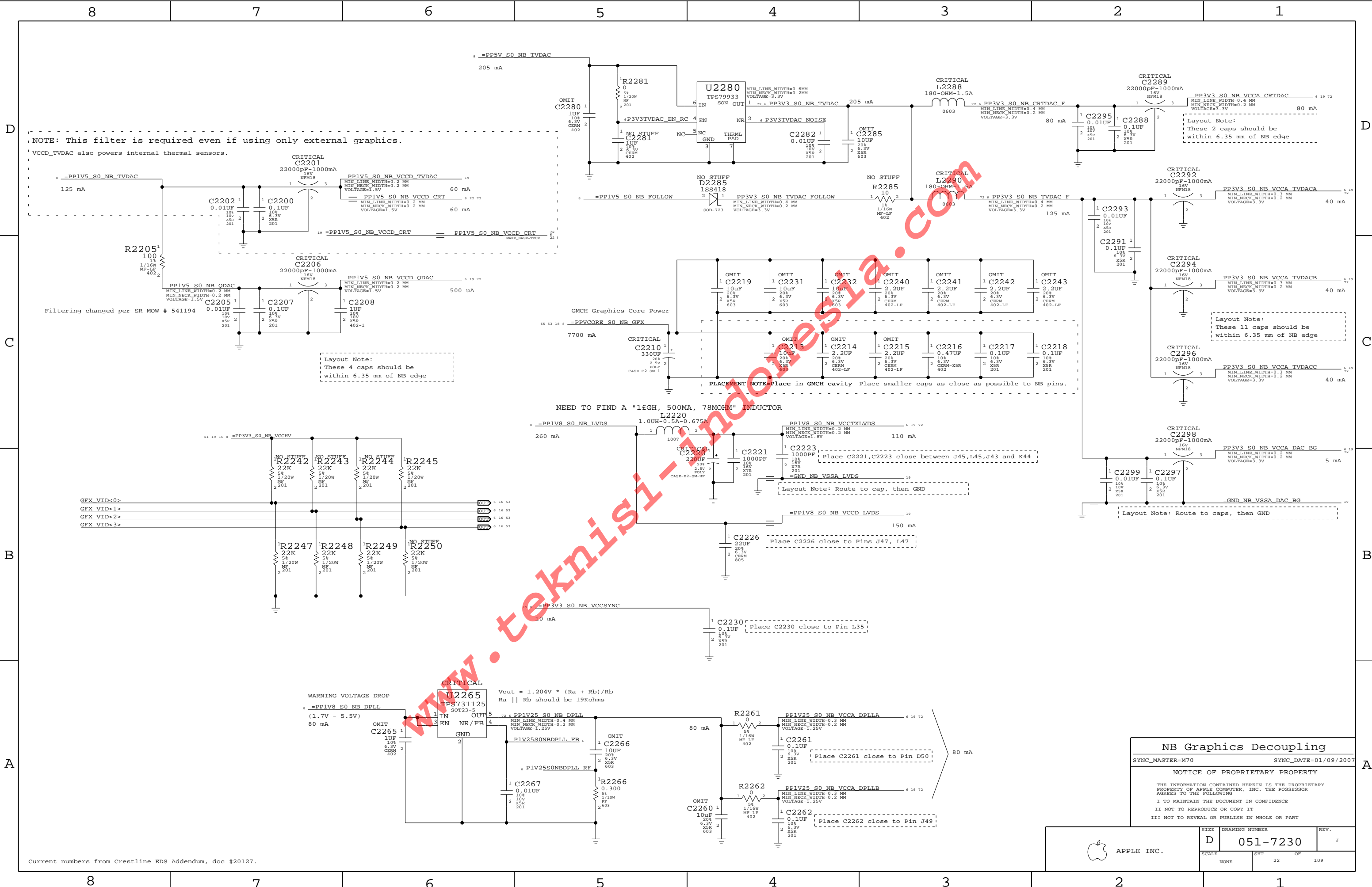


Current numbers from Crestline EDS Addendum, doc

NB Standard Decoupling		
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SCALE	SHT	OF
NONE	21	109



NOTE: This filter is required even if using only external graphics.
VCCD_TVDC also powers internal thermal sensors.

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

Layout Note:
These 11 caps should be
within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

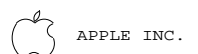
Place C2226 close to Pins J47, L47

Place C2230 close to Pin L35

Place C2261 close to Pin D50

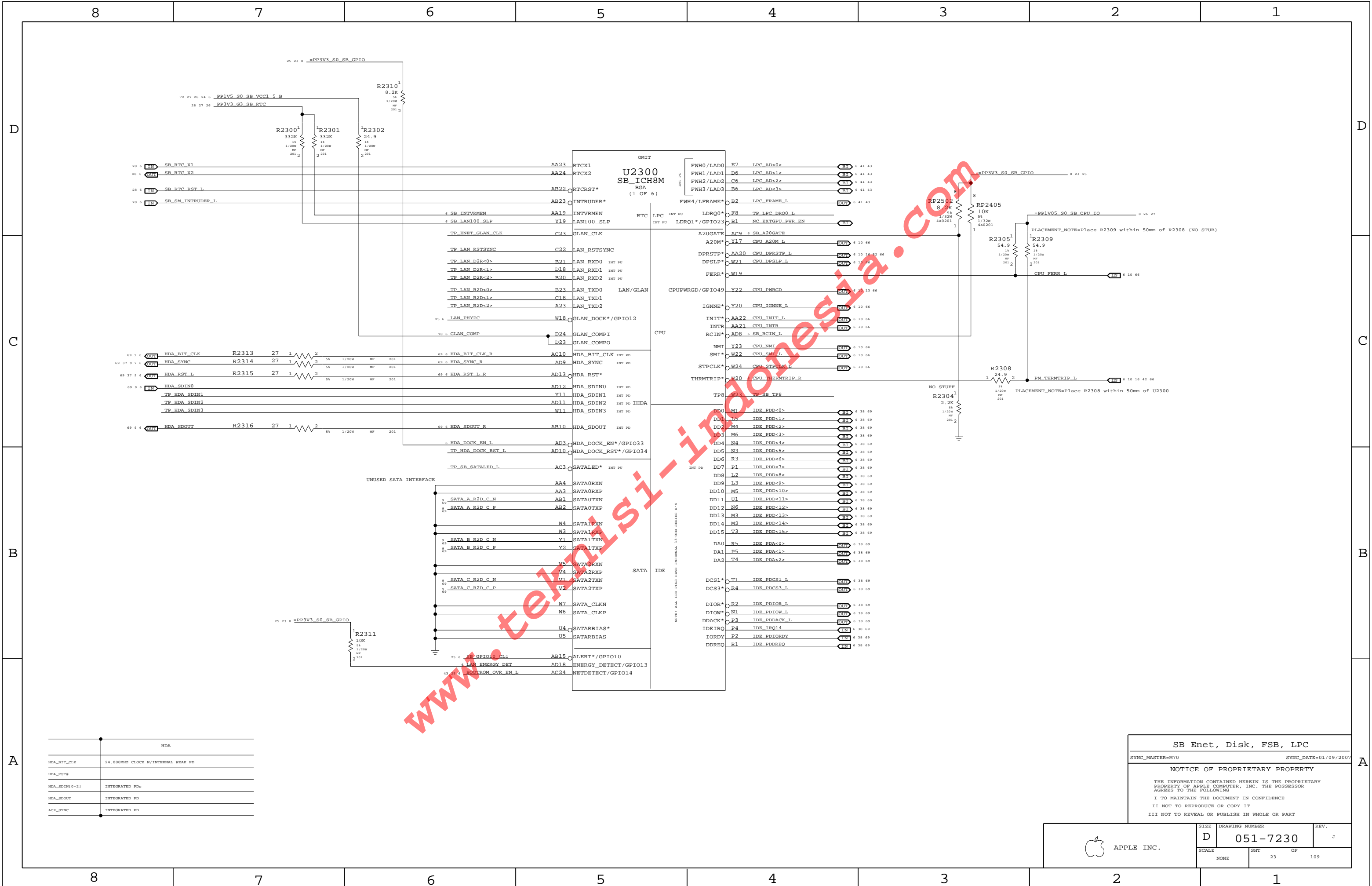
Place C2262 close to Pin J49

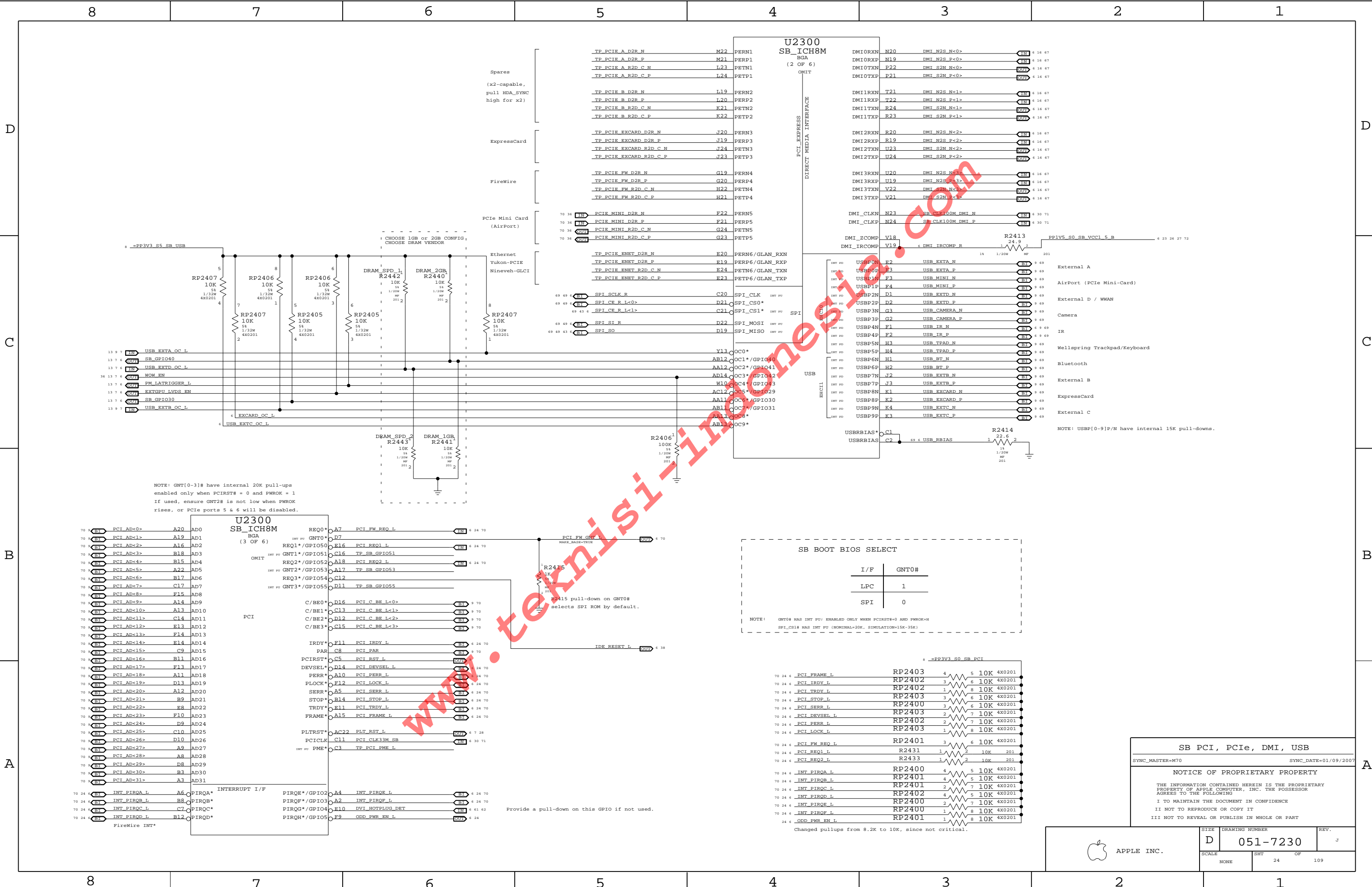
NB Graphics Decoupling
SYNC_MASTER=M70 SYNC_DATE=01/09/2007
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SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT	OF
NONE	22	109





SB BOOT BIOS SELECT		
I/F	GNT0#	
LPC	1	
SPI	0	

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST# = 0 AND PWROK = H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB PCI, PCIe, DMI, USB

SYNC_MASTER=M70

SYNC_DATE=01/09/2007

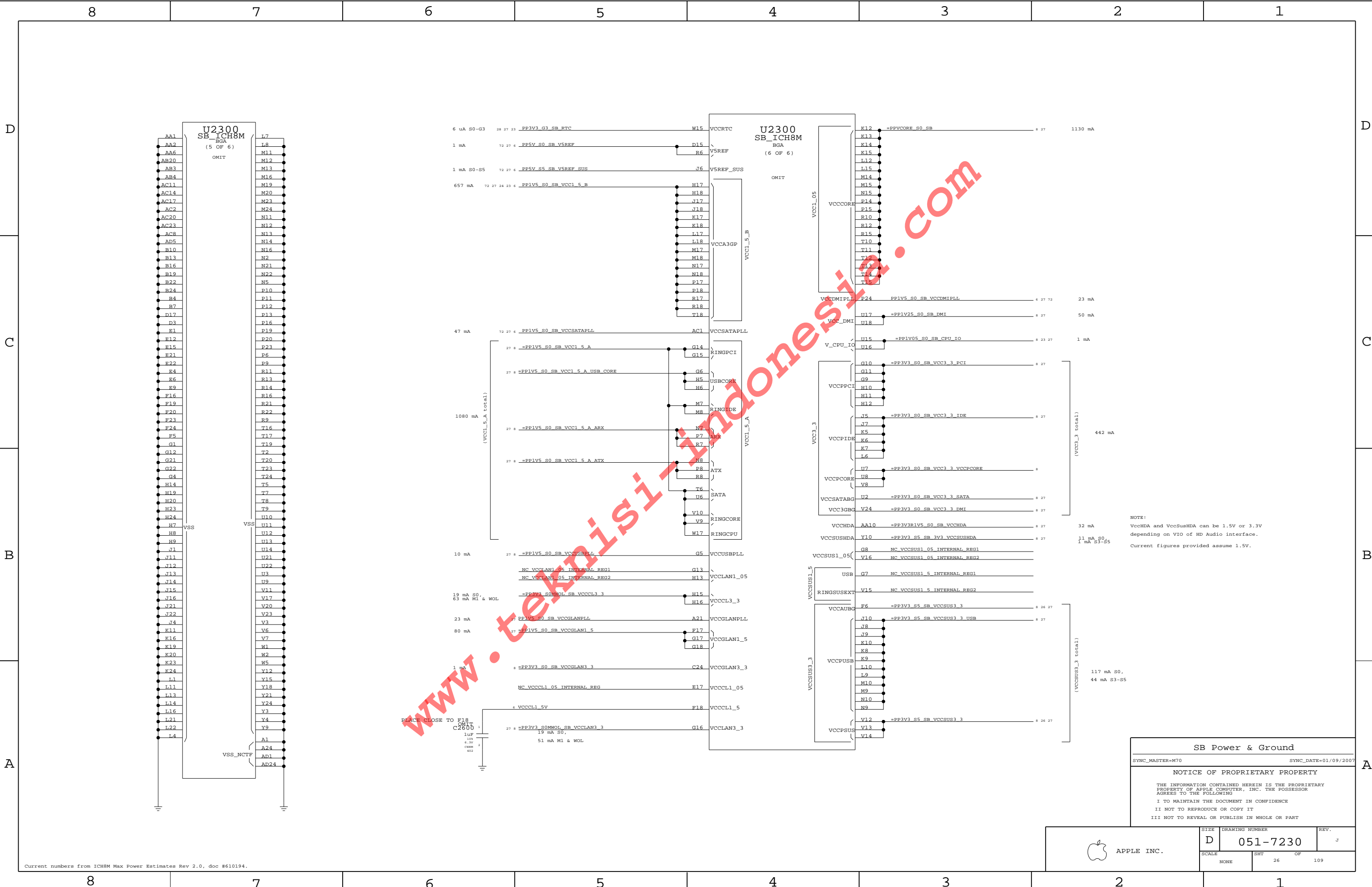
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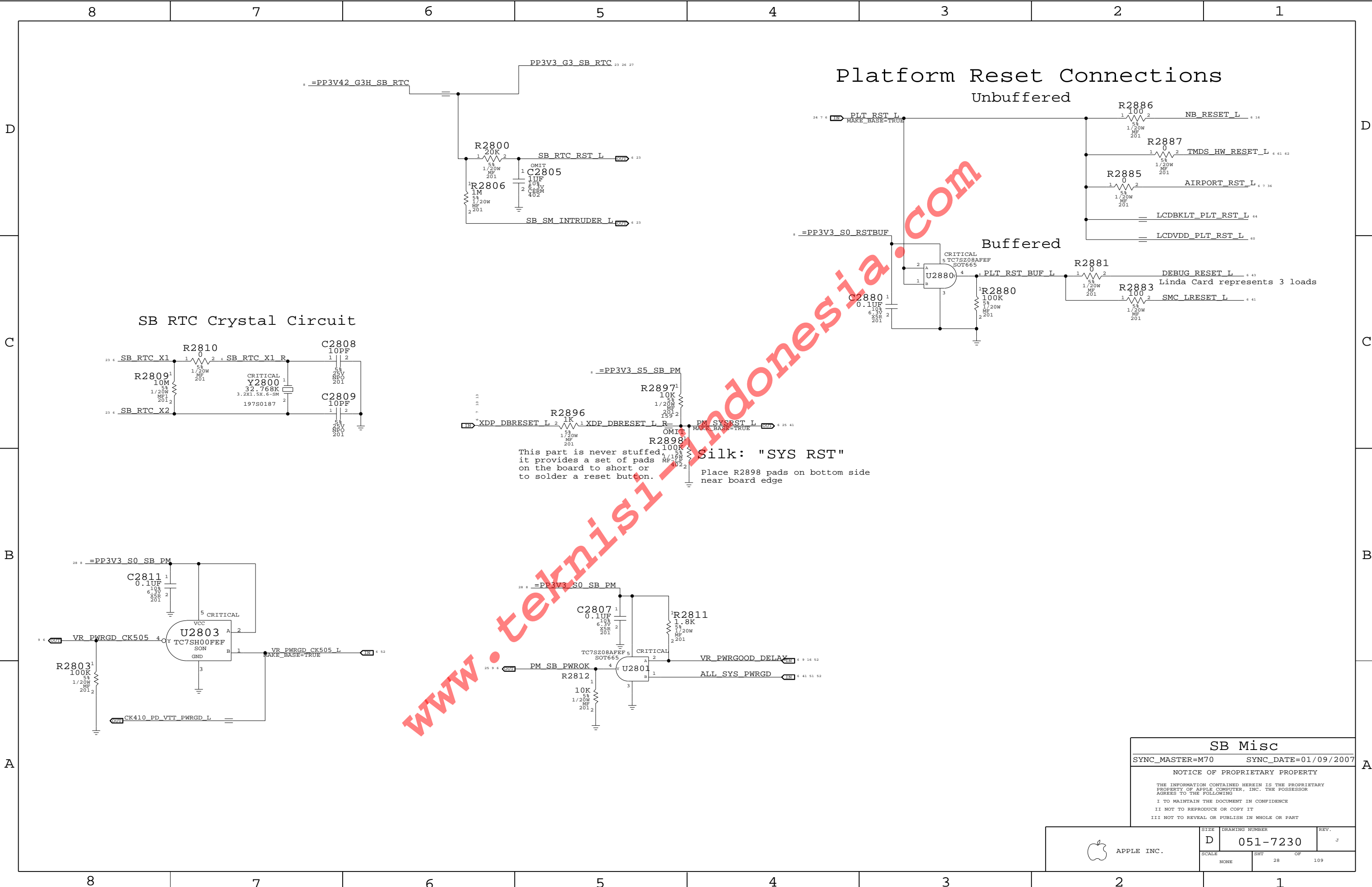
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



www.technical-indonesia.com

SB Power & Ground	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007
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	D	051-7230	J
SCALE		SHT	OF
NONE		26	109



www.ternisia.com

Platform Reset Connections

Unbuffered

Buffered

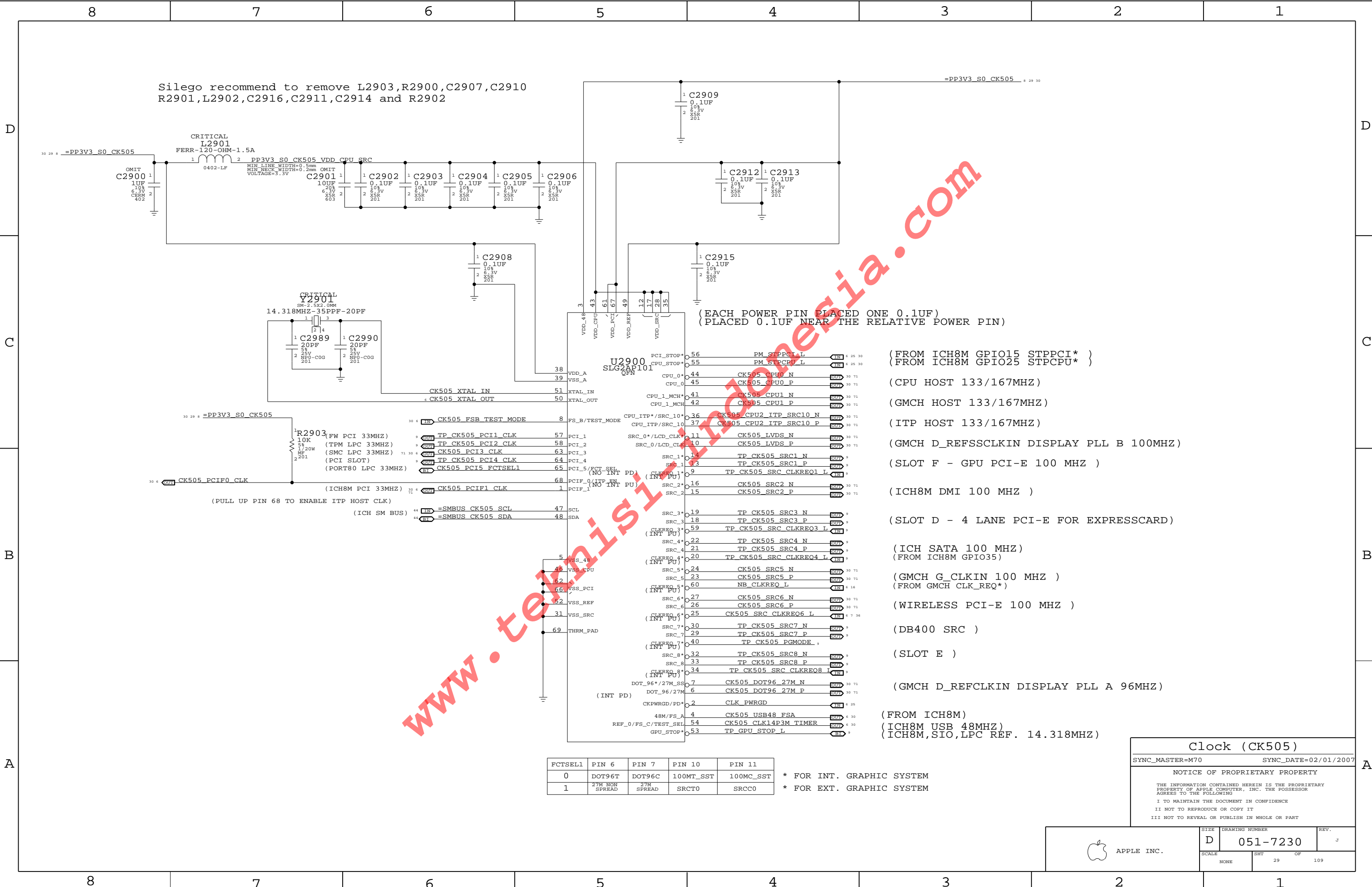
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

Place R2898 pads on bottom side near board edge

SB Misc	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007
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SCALE		SHT	OF
NONE		28	109



Silego recommend to remove L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

CRITICAL
L2901
FERR-120-OHM-1.5A
0402-LF
PP3V3_S0_CK505 VDD_CPU_SRC
MIN LINE WIDTH=0.5mm
MIN NECK WIDTH=0.2mm OMIT
VOLTAGE=3.3V

CRITICAL
Y2901
SM-2.5X2.0MM
14.318MHZ-35PPF-20PF

R2903 (FW PCI 33MHZ)
(TPM LPC 33MHZ)
(SMC LPC 33MHZ)
(PCI SLOT)
(PORT80 LPC 33MHZ)

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)
(ICH8M PCI 33MHZ)
(ICH SM BUS)

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

(FROM ICH8M GPIO15 STPPCI*)
(FROM ICH8M GPIO25 STPCPU*)
(CPU HOST 133/167MHZ)
(GMCH HOST 133/167MHZ)
(ITP HOST 133/167MHZ)
(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
(SLOT F - GPU PCI-E 100 MHZ)
(ICH8M DMI 100 MHZ)
(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
(ICH SATA 100 MHZ)
(FROM ICH8M GPIO35)
(GMCH G_CLKIN 100 MHZ)
(FROM GMCH CLK_REQ*)
(WIRELESS PCI-E 100 MHZ)
(DB400 SRC)
(SLOT E)
(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
(FROM ICH8M)
(ICH8M USB 48MHZ)
(ICH8M,SIO,LPC REF. 14.318MHZ)

Clock (CK505)

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

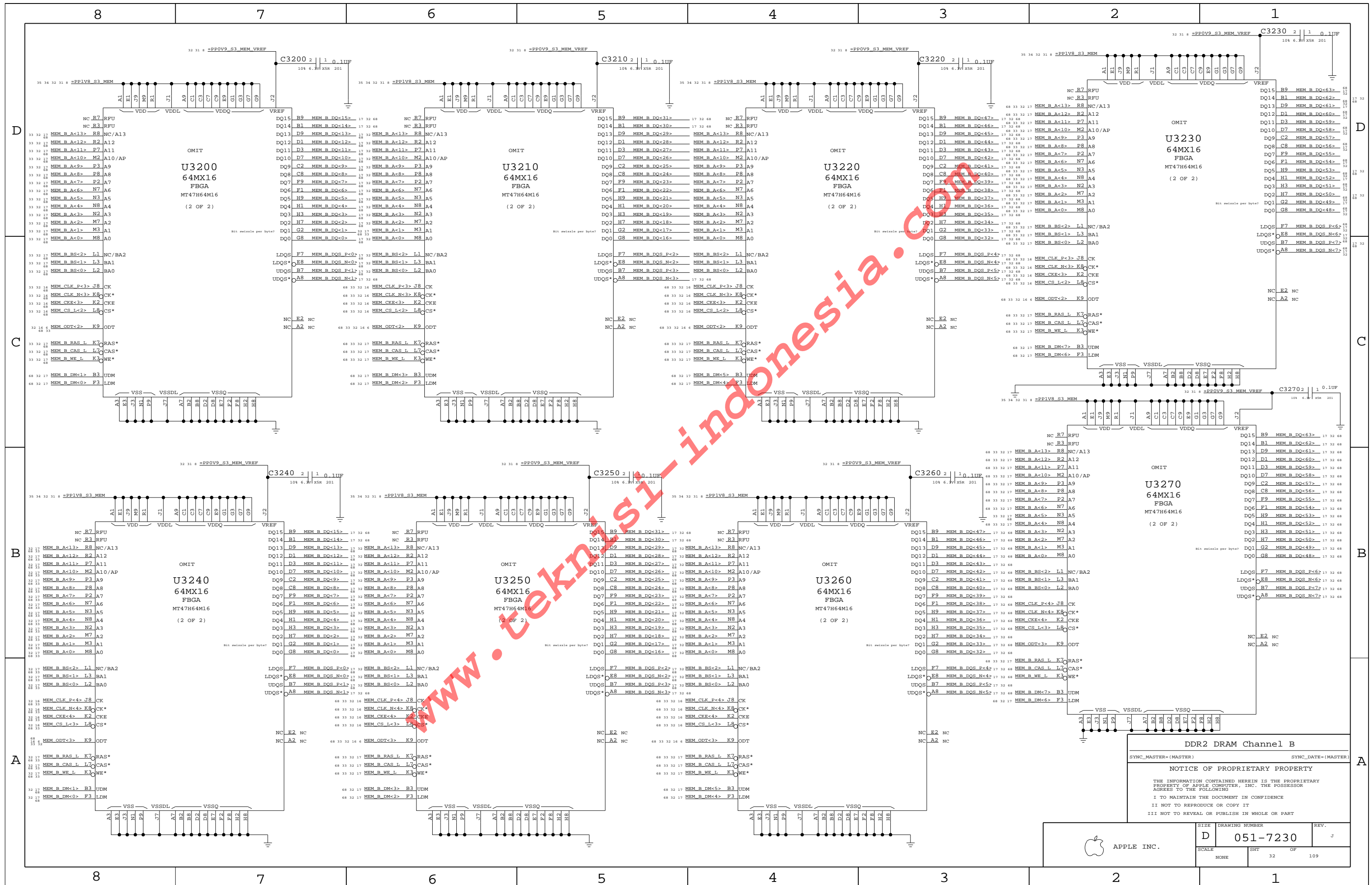
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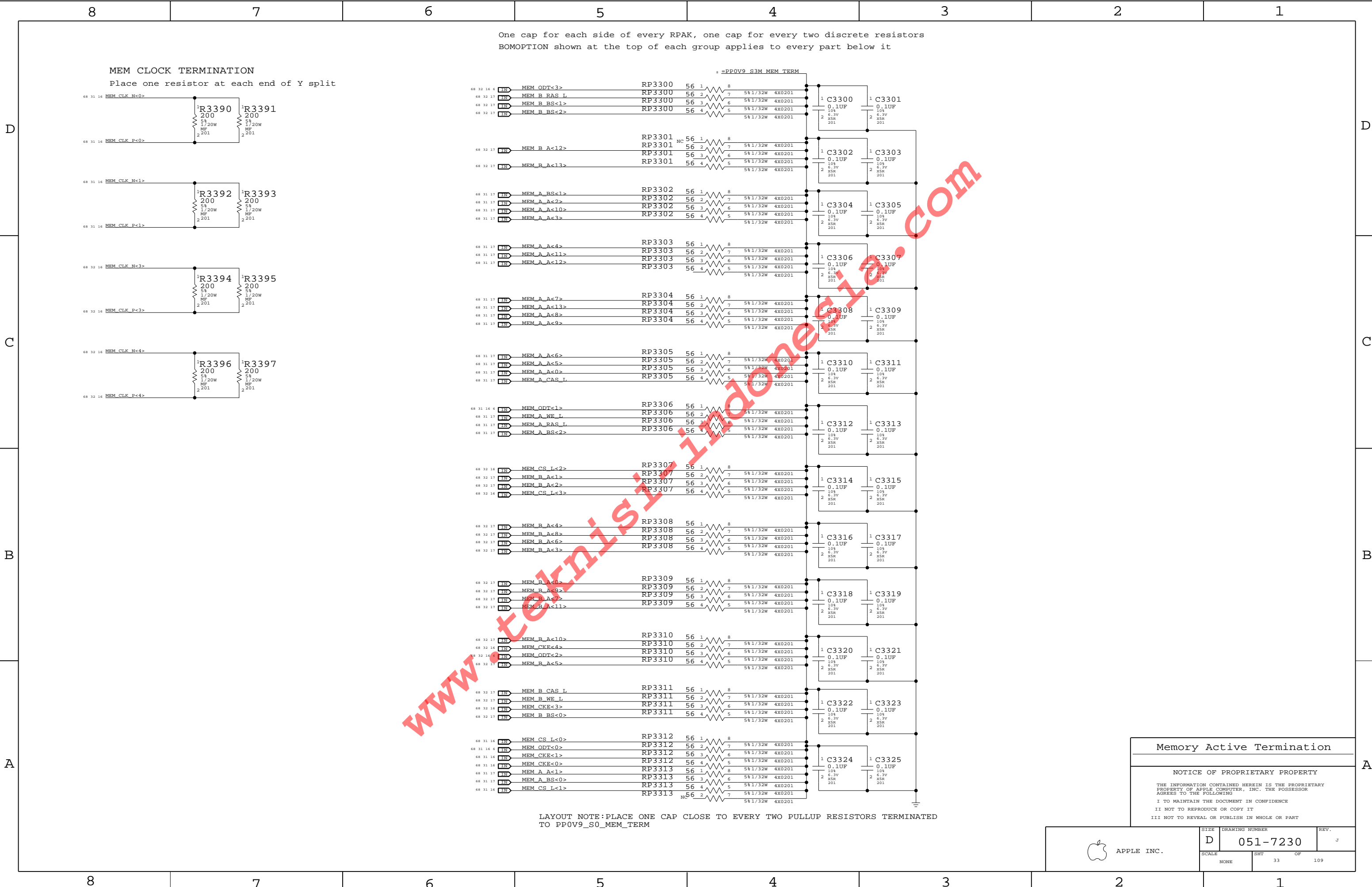
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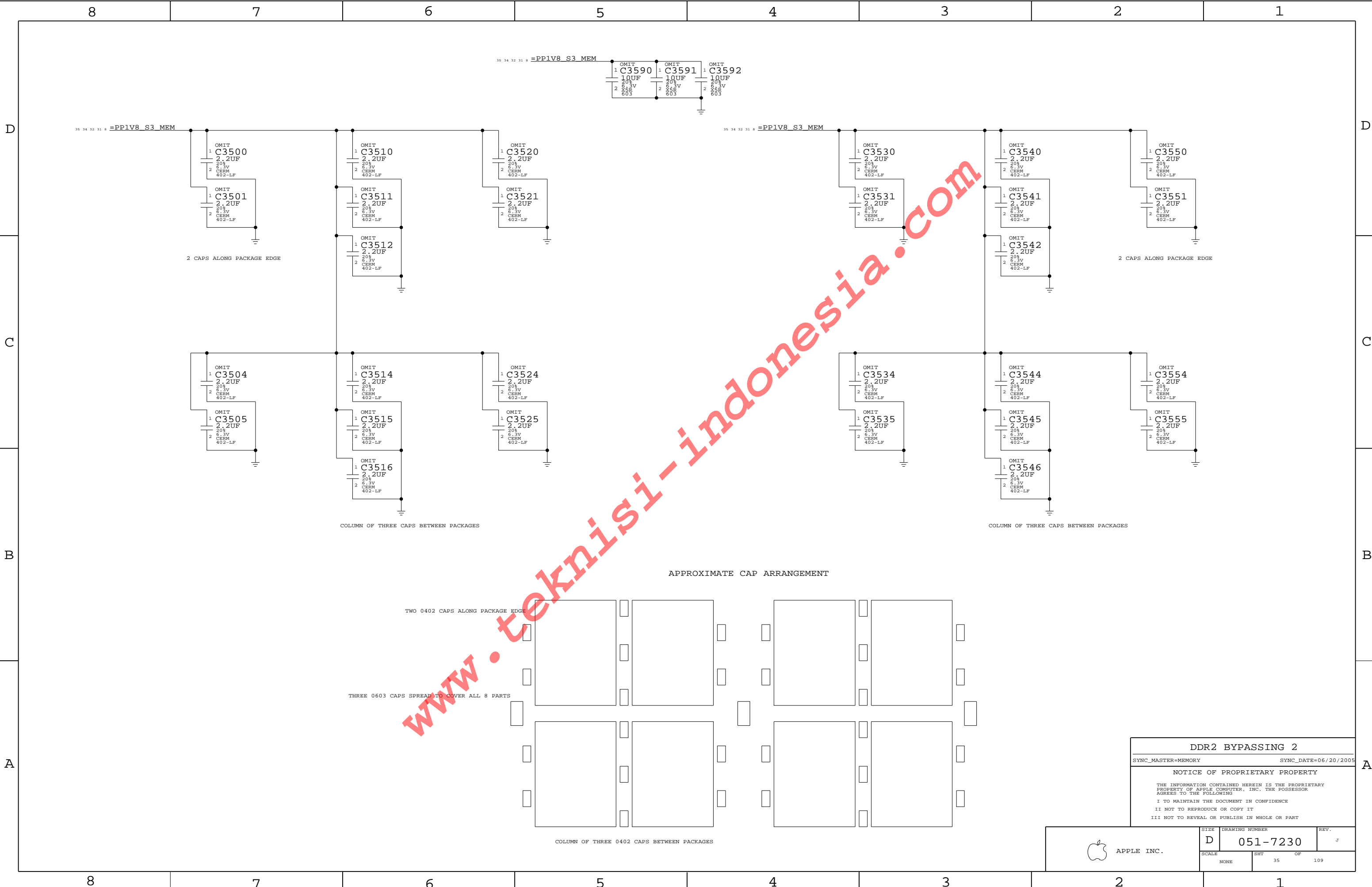


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT	OF
NONE	29	109

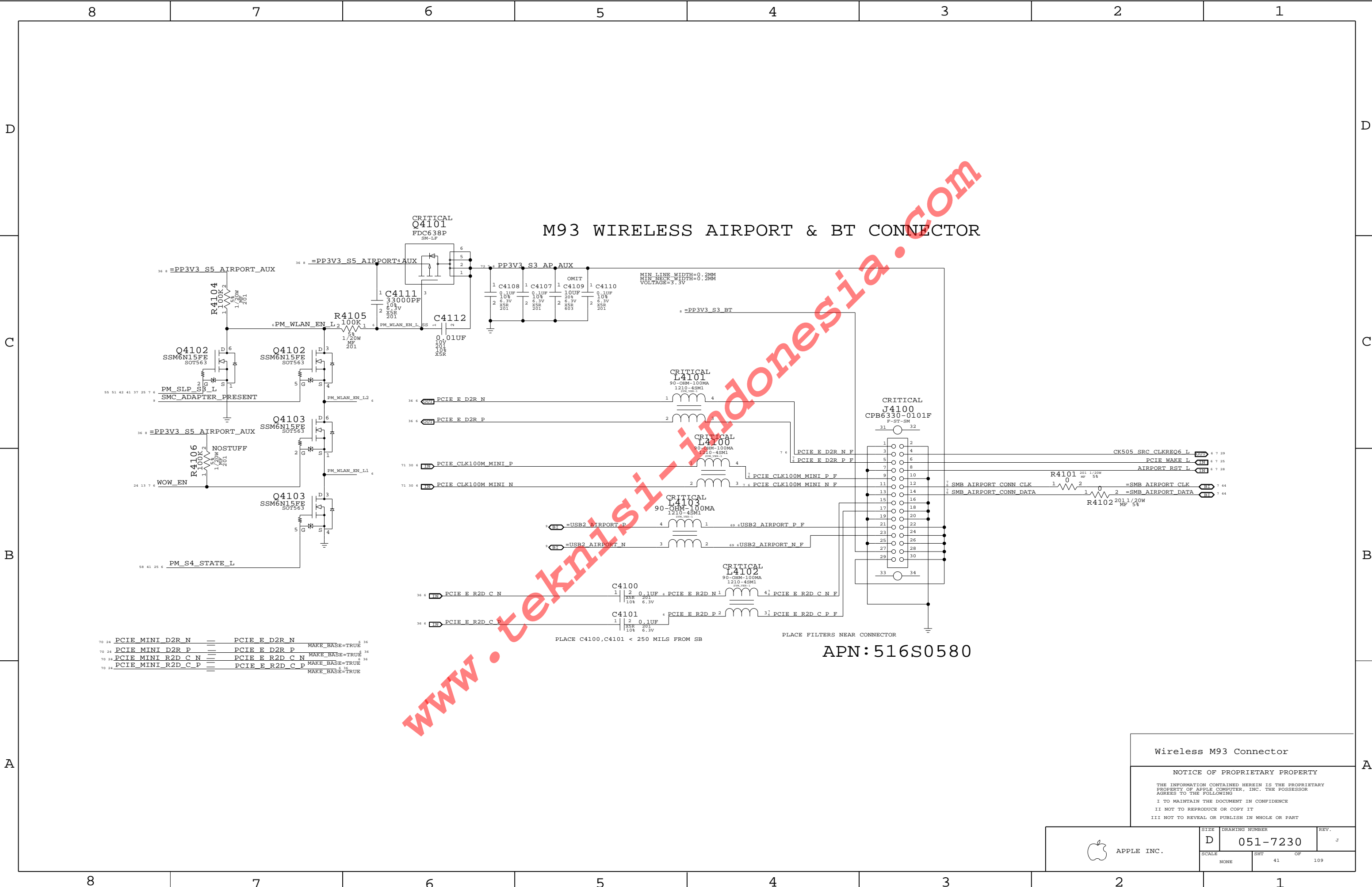






DDR2 BYPASSING 2
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005
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SCALE		SHT	OF
NONE		35	109



M93 WIRELESS AIRPORT & BT CONNECTOR

APN: 516S0580

Wireless M93 Connector

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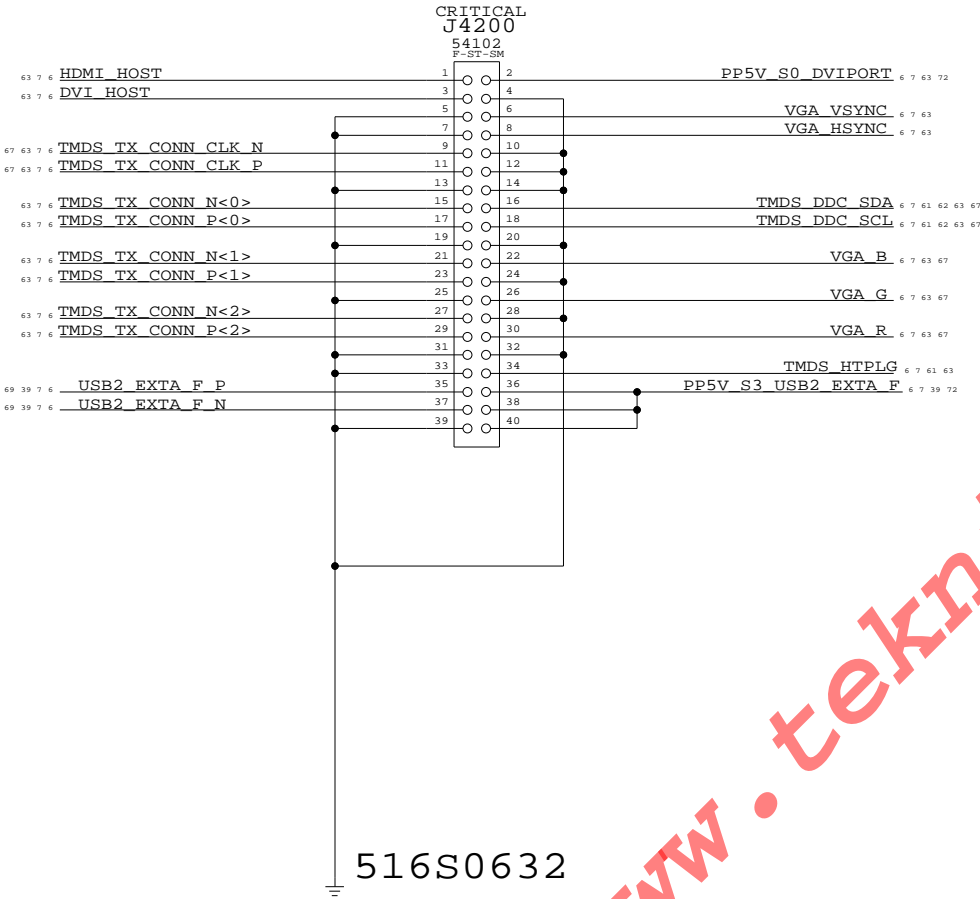
APPLE INC.

SIZE DRAWING NUMBER REV.

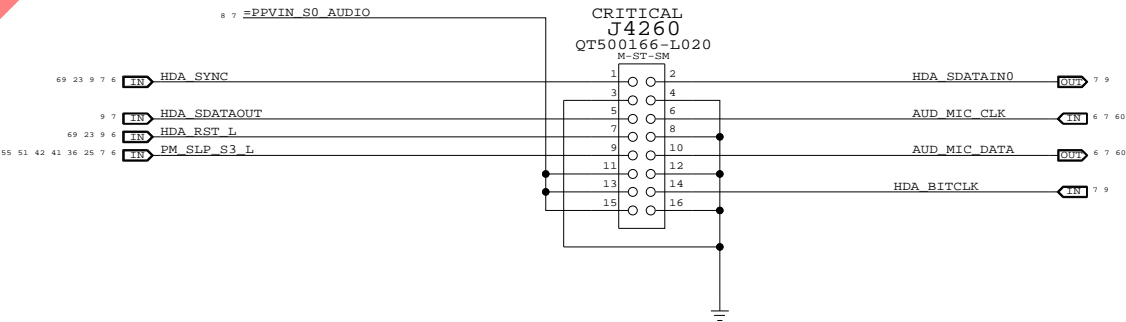
D 051-7230 J

SCALE NONE SHT 41 OF 109

Micro DVI, USB, to RIO Hatch Assembly

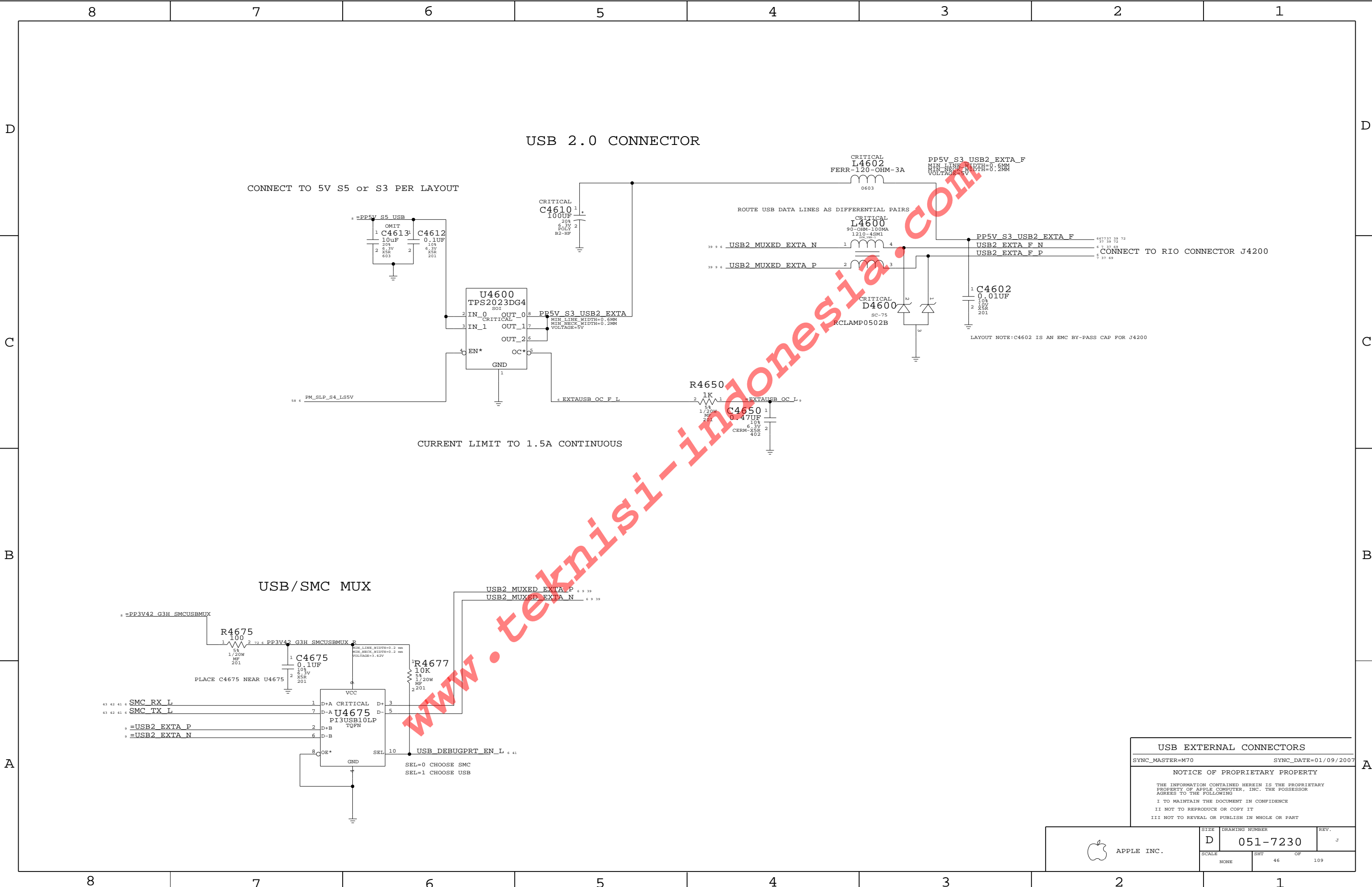


Audio Connector



Hatch and Audio Connectors	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
SCALE		SHT	OF
NONE		42	109



USB EXTERNAL CONNECTORS

SYNC_MASTER=M70

SYNC_DATE=01/09/2007


NOTICE OF PROPRIETARY PROPERTY

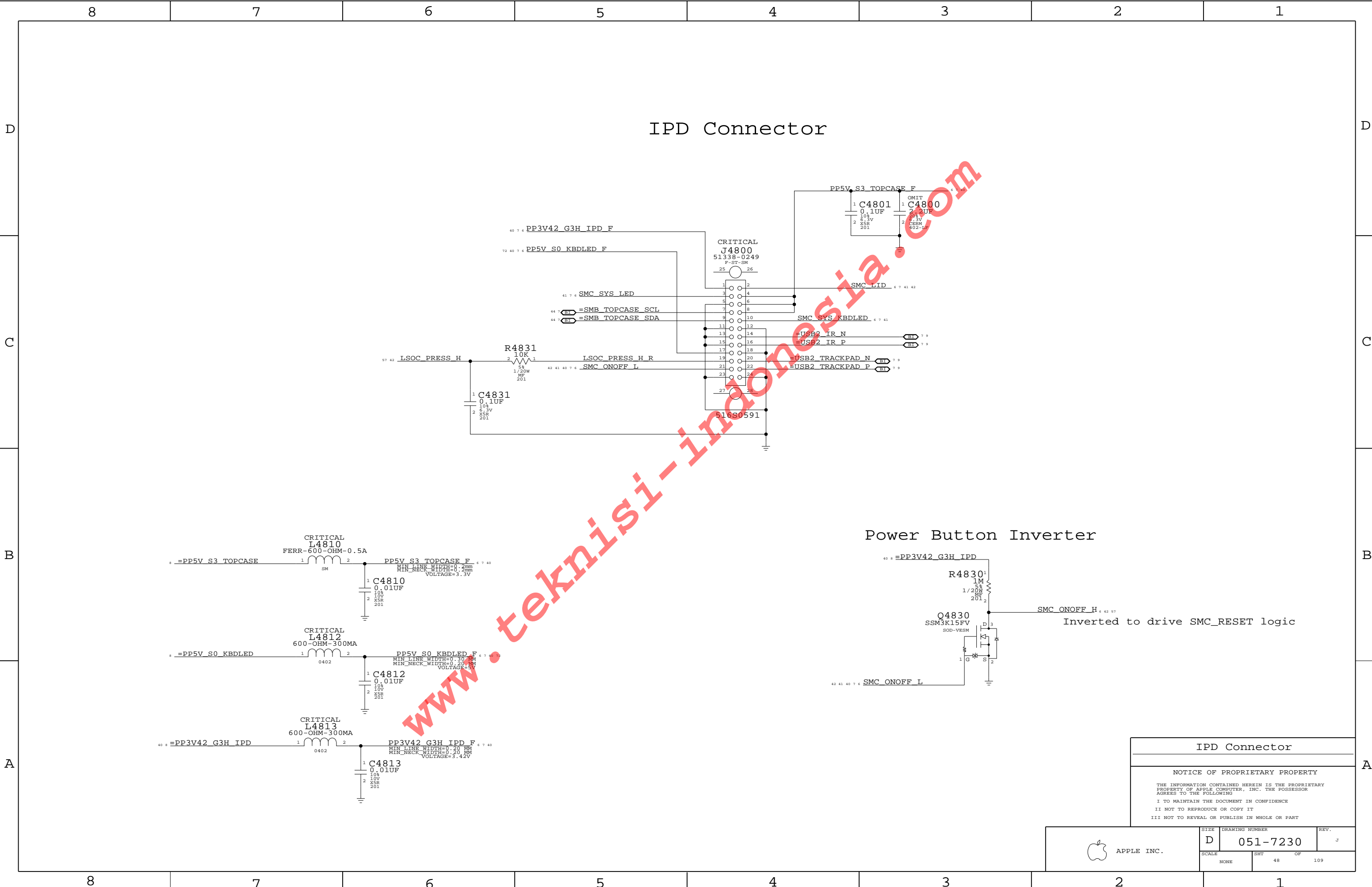
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	D	051-7230	J
SCALE		SHT	OF
NONE		46	109



IPD Connector

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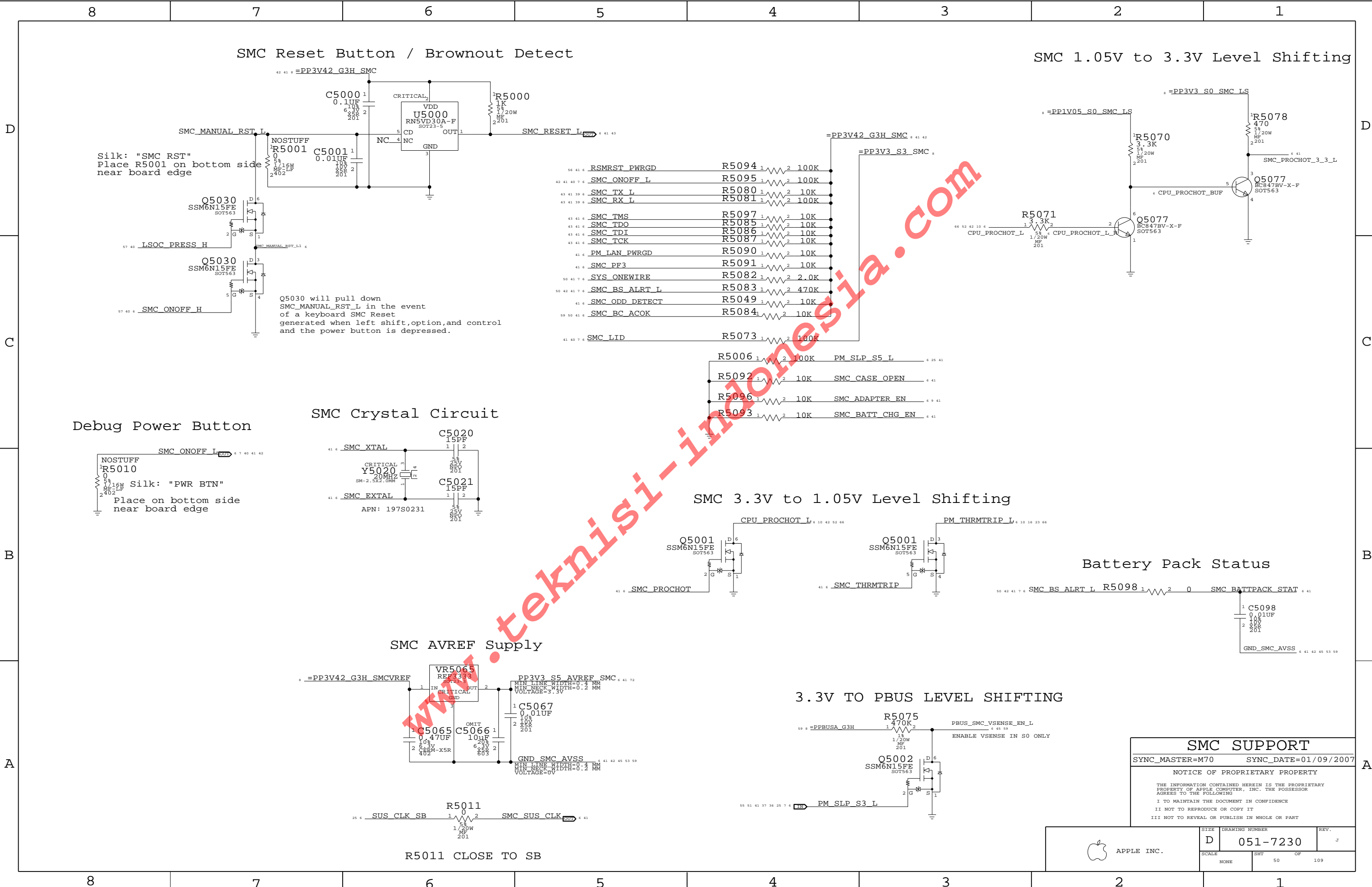
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	D	051-7230	J
SCALE		SHT	OF
NONE		48	109



SMC Reset Button / Brownout Detect

SMC 1.05V to 3.3V Level Shifting

Silk: "SMC RST"
Place R5001 on bottom side
near board edge

Q5030 will pull down
SMC_MANUAL_RST_L in the event
of a keyboard SMC Reset
generated when left shift,option,and control
and the power button is depressed.

Debug Power Button

Silk: "PWR BTN"
Place on bottom side
near board edge

SMC Crystal Circuit

APN: 197S0231

SMC 3.3V to 1.05V Level Shifting

Battery Pack Status

SMC AVREF Supply

3.3V TO PBUS LEVEL SHIFTING

R5011 CLOSE TO SB

SMC SUPPORT

SYNC_MASTER=M70

SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

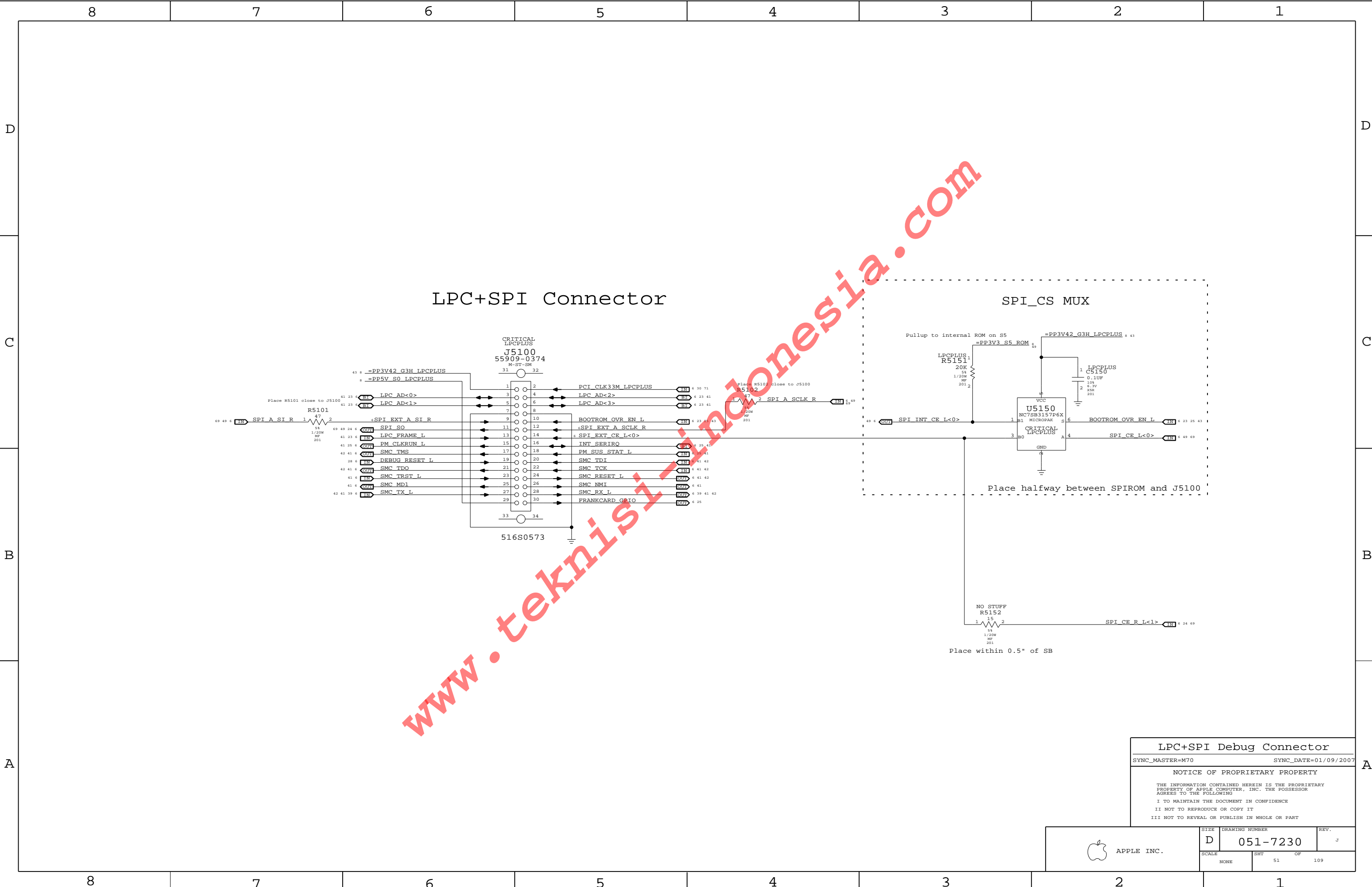
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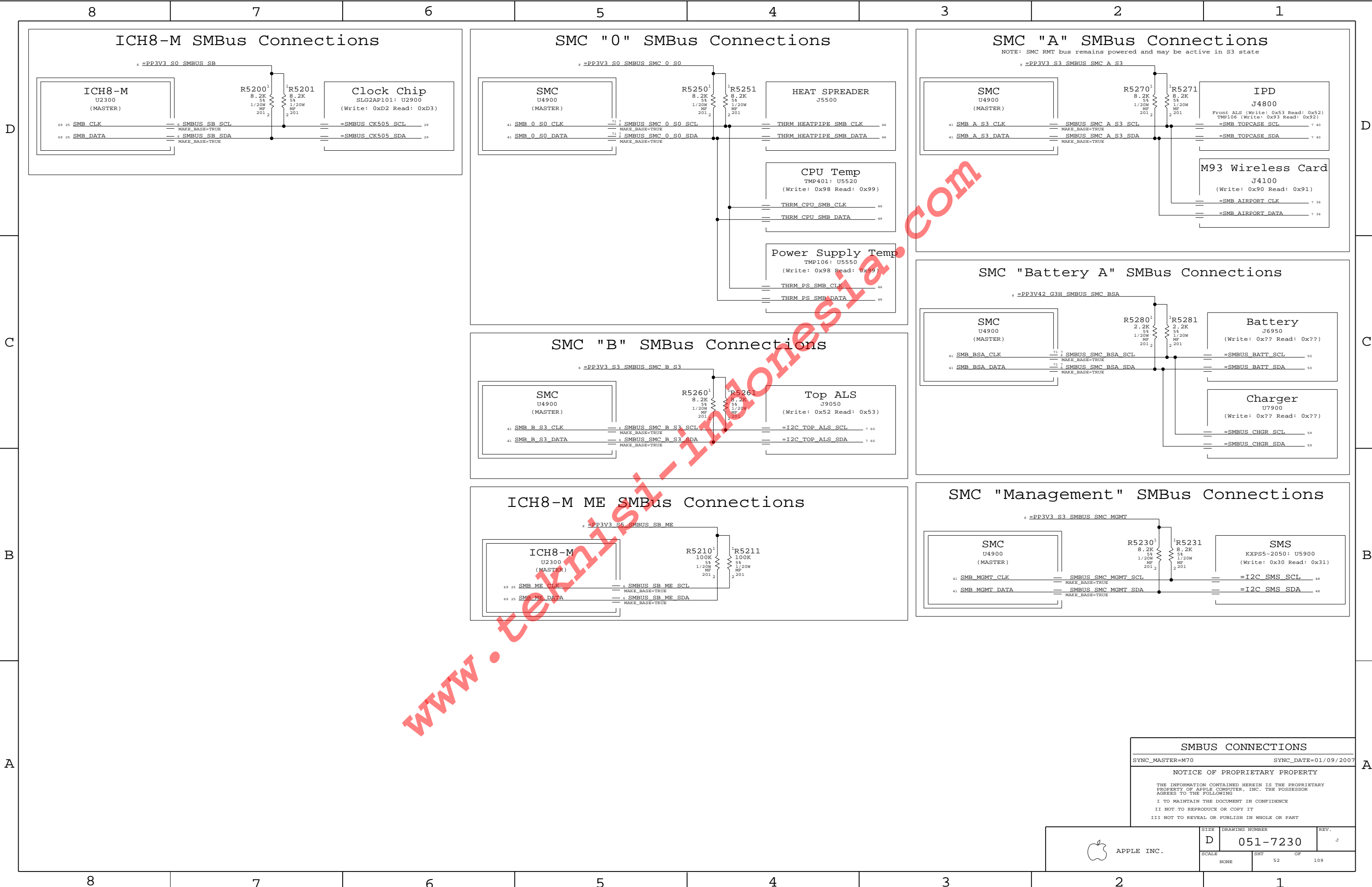
APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7230		J
SCALE		SHT	OF	109
NONE		50		



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LPC+SPI Debug Connector
SYNC_MASTER=M70 SYNC_DATE=01/09/2007
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
SCALE		SHT	OF
NONE		51	109



SMBUS CONNECTIONS

SYNC_MASTER=M70

SYNC_DATE=01/09/2007

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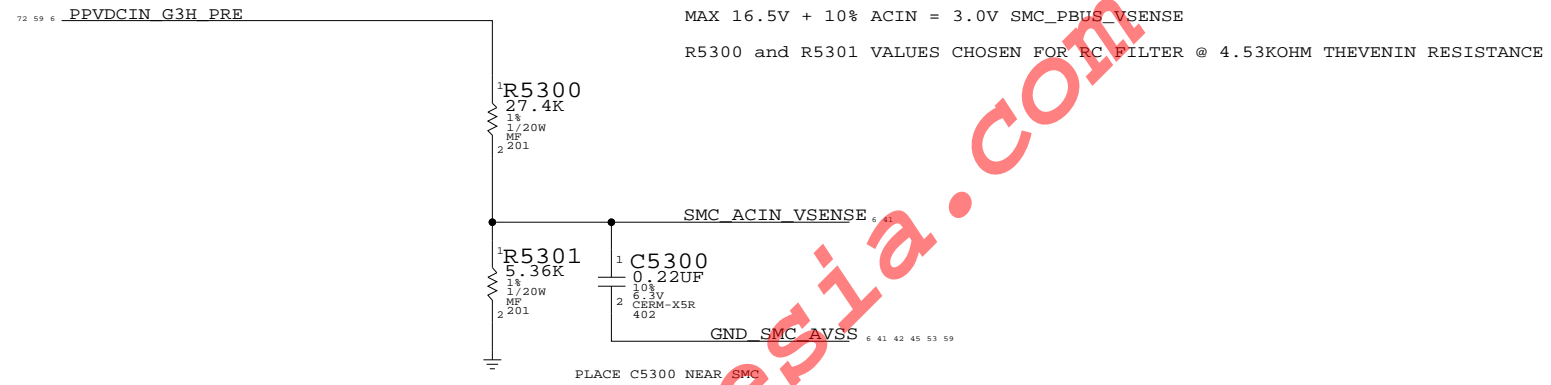
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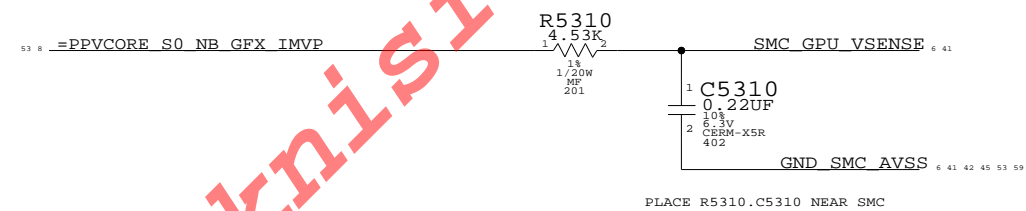
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7230		J
SCALE		NONE	SHT 52 OF 109	

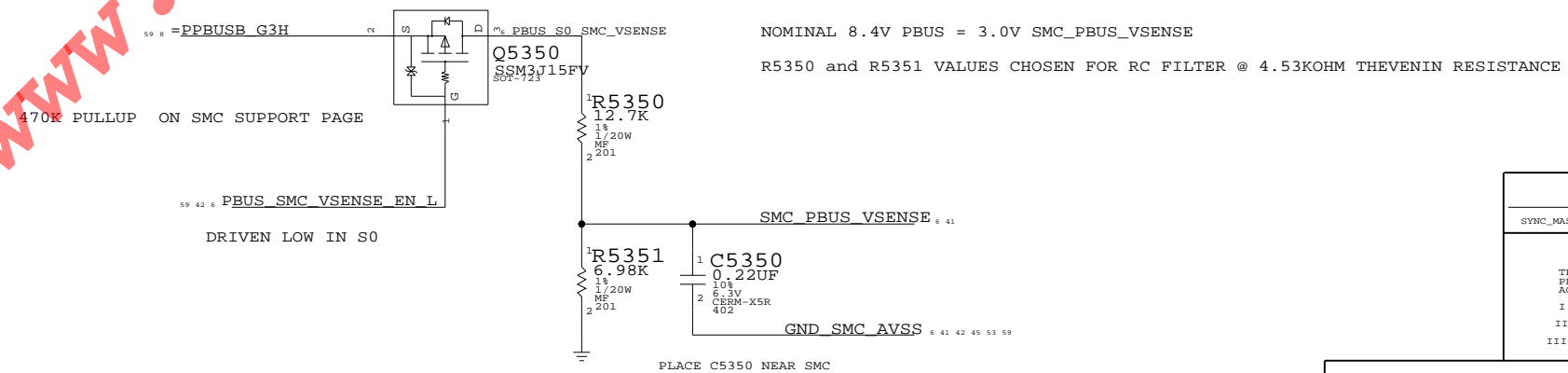
ACIN VOLTAGE SENSE




GPU VOLTAGE SENSE

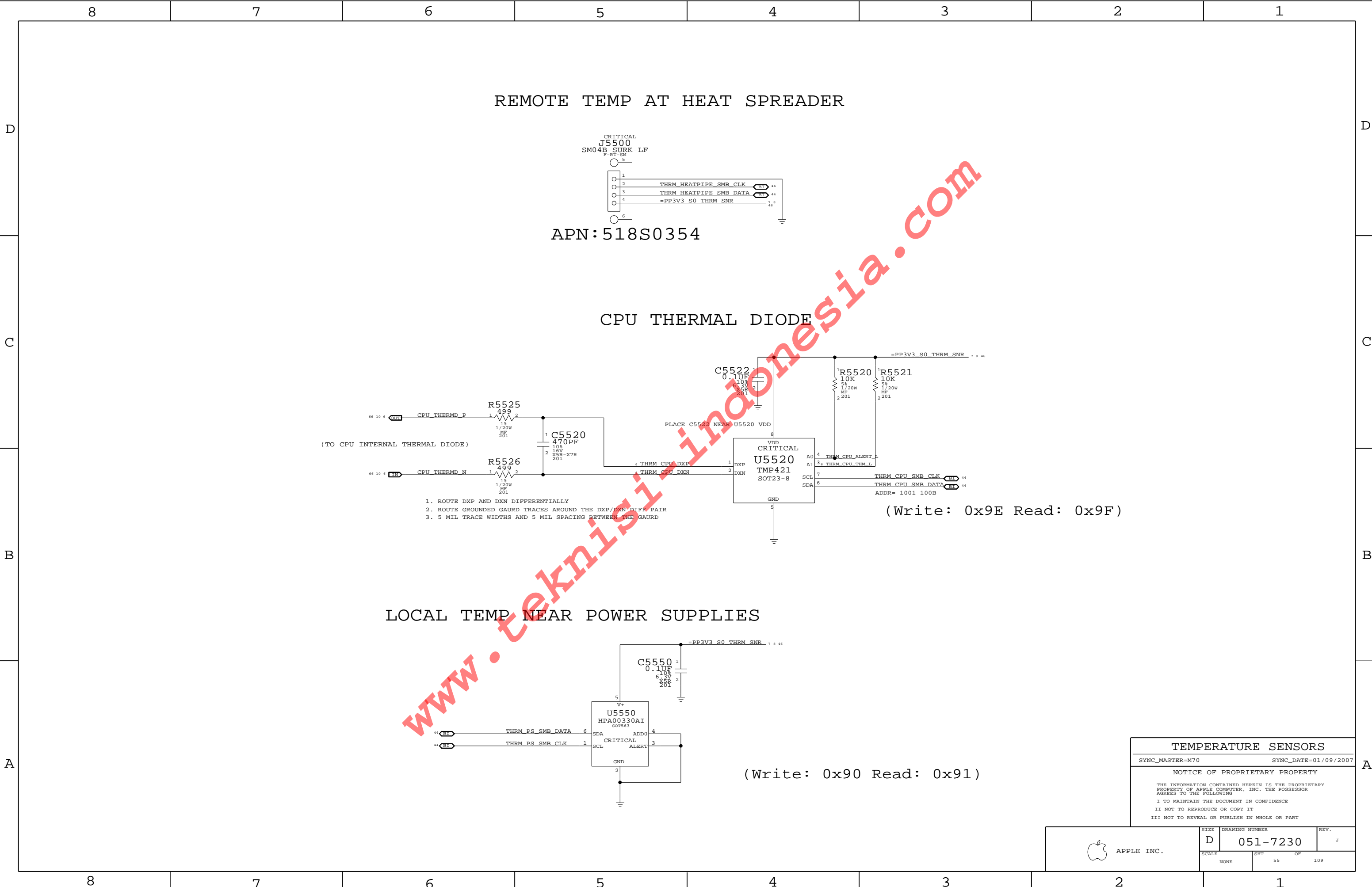


PBUS VOLTAGE SENSE



Voltage Sensors	
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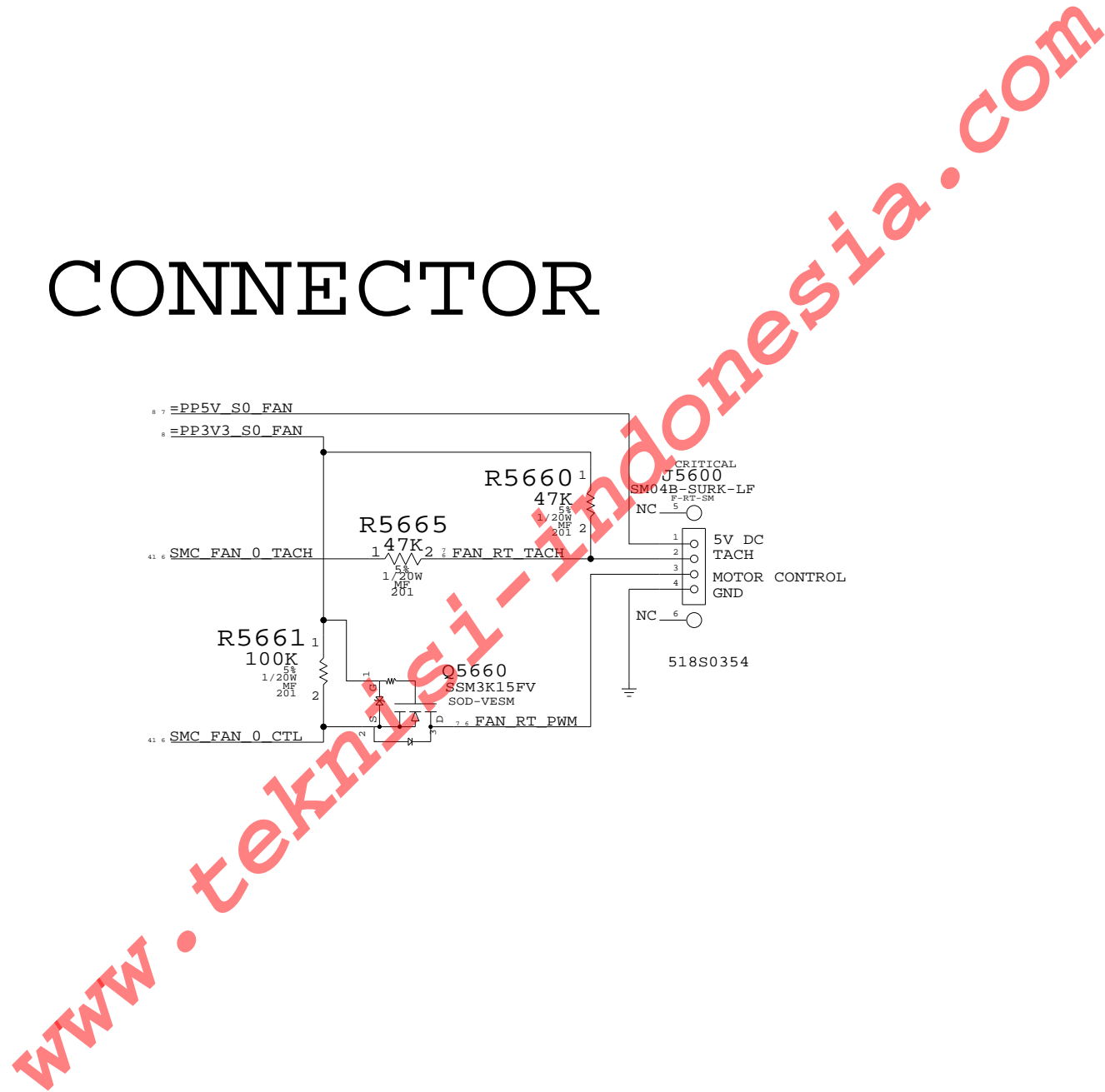
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
	SCALE	SHT OF	
	NONE	53 109	





CONNECTOR

The schematic diagram illustrates the electrical connections for a fan motor control system. Key components and connections include:

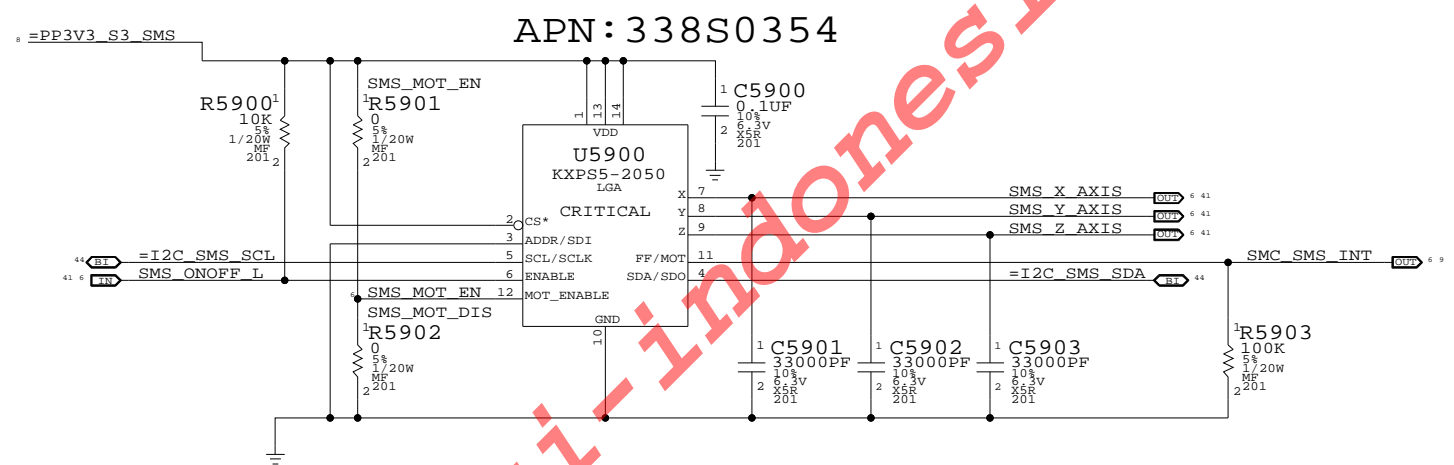
- Power Supplies:** PP5V_S0_FAN (5V) and PP3V3_S0_FAN (3.3V) provide power to the circuit.
- Resistors:** R5660 (47K, 1/20W) and R5661 (100K, 1/20W) are used for signal conditioning.
- Diode:** Q5660 (SSM3K15FV, SOD-VESM) is a Schottky diode used for protection.
- Connectors:** The circuit is connected to a 5V DC supply, a TACH (tachometer) input, and a MOTOR CONTROL output.
- Motor:** The motor is labeled 518S0354.



 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
	SCALE	SHT	OF
	NONE	56	109

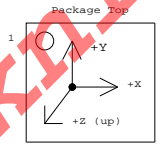
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
	SCALE	SHT	OF
	NONE	56	109

SUDDEN MOTION SENSOR

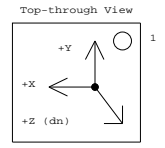


I2C addresses:
ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when
placed on board top-side:



Desired orientation when
placed on board bottom-side:



Sudden Motion Sensor (SMS)

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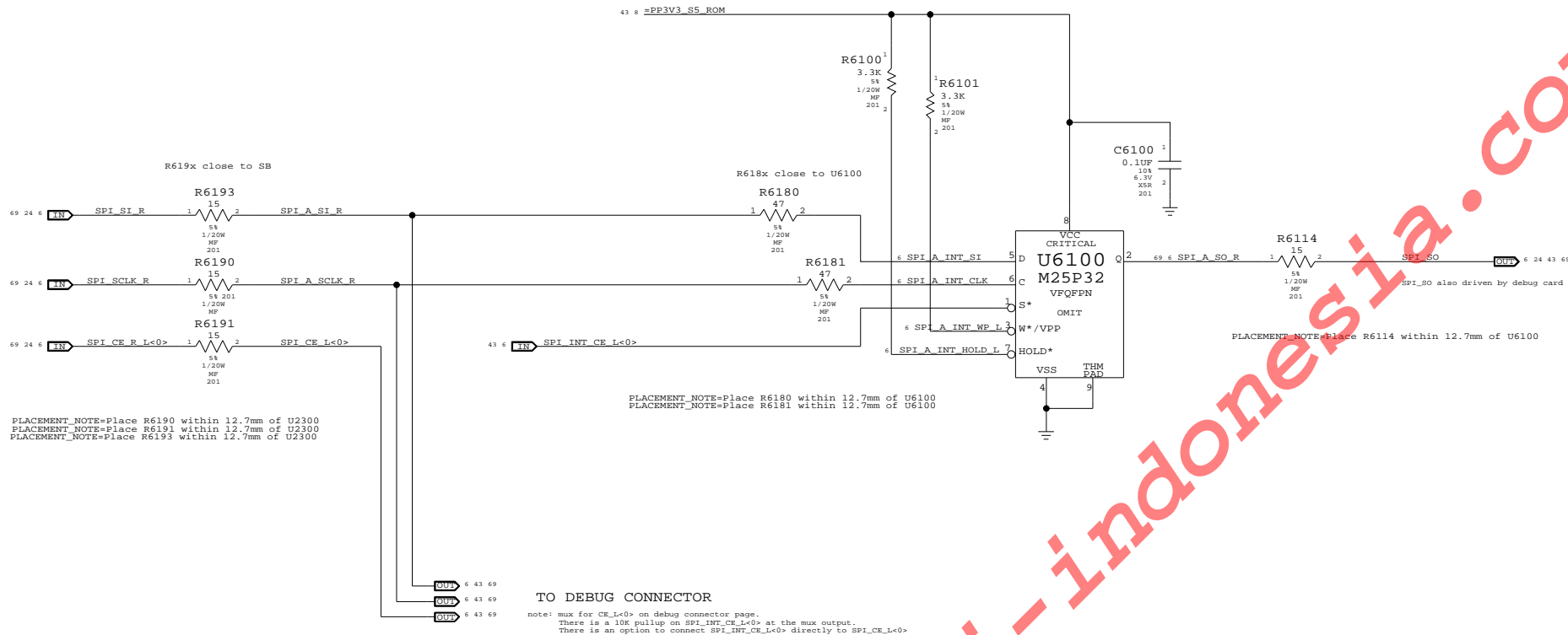
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SCALE		SHT	OF
NONE		59	109

SPI ROM



SPI ROMs

SYNC_MASTER=WFERRY

SYNC_DATE=04/26/2006

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7230

REV.

J

SCALE

NONE

SHT

61

OF

109

[illegible]

CRITICAL

J6900
WTB-PWR-M82
M-RT-SM

L6900
FERR-50-OHM

C6900
0.01UF
10K
25V
X7S
402

SM-BLIF

6 BATT POS

6 50 50

SMC_BS_ALRT_L

=SMBUS_BATT_SDA

=SMBUS_BATT_SCL

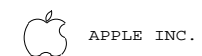
6 7 41 42

44

44

518S0540

DC-In & Battery Connectors	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007
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SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT OF	
NONE	69	109

D



APPLE INC.

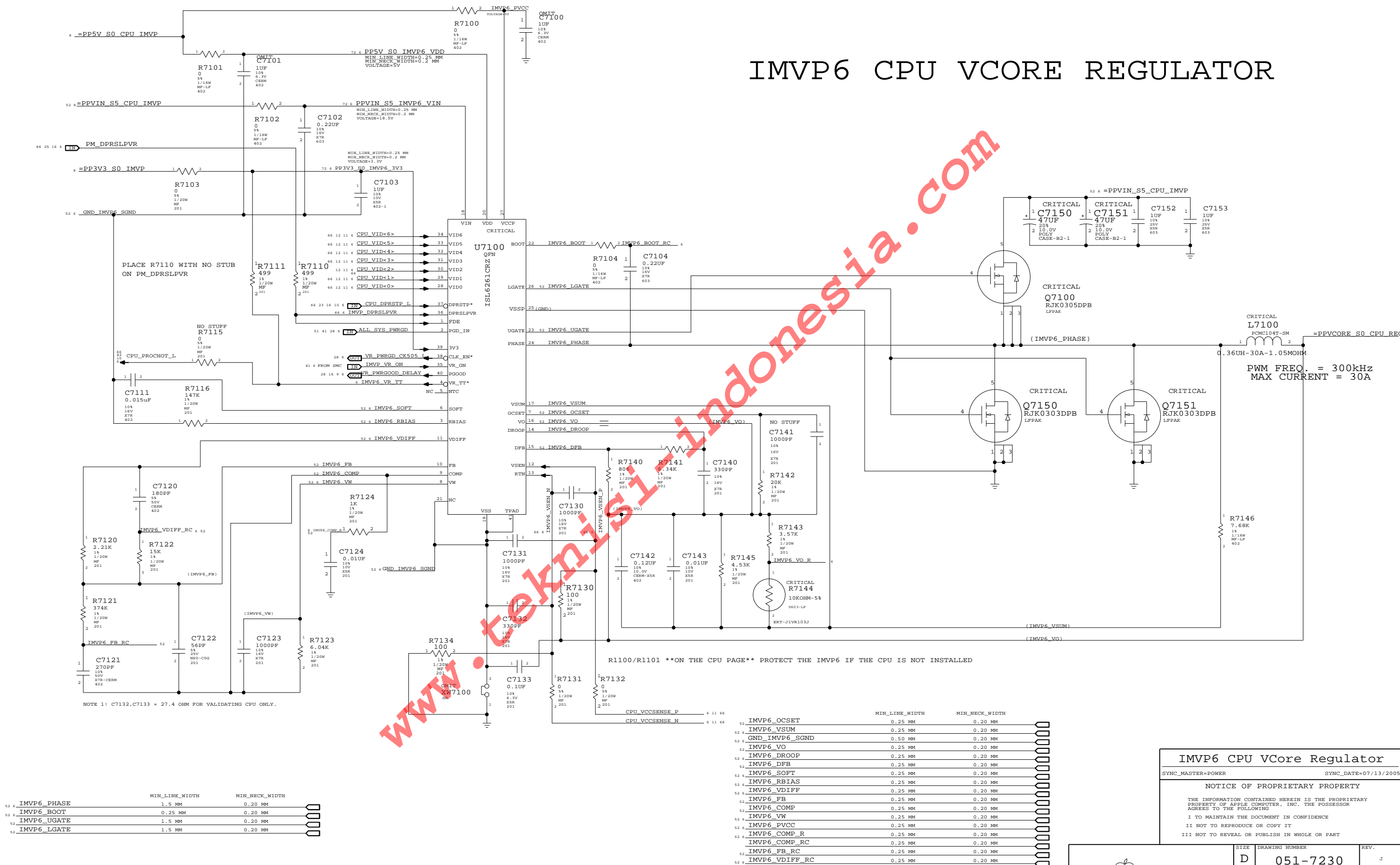
SIZE	DRAWING NUMBER	REV.
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D	051-7230	J
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SCALE	SHT	OF
NONE	70	109

STUFF R7013,R7014 and UNSTUFF U7002,C7001,C7002
TO USE WIRE-AND OF ALL PGOODS INSTEAD OF TPS3808

IMVP6 CPU VCore REGULATOR



D



C

C

B

B

A

A

```

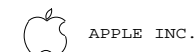
NOTE: VID<4> is tied to GND
  4 3 2 1 0 VOLTAGE
VID 0 0 0 0 0 1.250V      Each step is 0.025V
VID 0 0 0 0 0 1 1.225V
VID 0 0 0 0 0 1 1 1.200V
VID 0 0 0 0 0 1 1 1.175V
VID 0 0 0 0 1 0 0 1.150V
VID 0 0 0 0 1 0 1 1.125V
VID 0 0 0 1 0 1 0 1.100V
VID 0 0 0 1 0 1 1 1.075V
VID 0 0 1 0 0 0 1 1.050V
VID 0 0 1 0 0 0 1 1.025V
VID 0 0 1 0 0 1 0 1.000V
VID 0 0 1 0 0 1 1 0.975V
VID 0 0 1 0 1 0 0 0.950V
VID 0 0 1 0 1 0 1 0.925V
VID 0 0 1 0 1 1 0 0.900V
VID 0 0 1 0 1 1 1 0.875V

```

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
53 6 GCORE_SW	0.6 MM	0.20 MM	1103
53 6 GCORE_BST	0.3 MM	0.20 MM	1104
53 6 GCORE_DRVH	0.6 MM	0.20 MM	1105
53 6 GCORE_DRVL	0.6 MM	0.20 MM	1106
53 6 GCORE_BST_D	0.3 MM	0.20 MM	1107
53 6 GND_GCORE_PGND	0.6 MM	0.20 MM	1108
53 6 GCORE_VDC_DIV	0.3 MM	0.20 MM	1109
53 6 GCORE_RAMP	0.3 MM	0.20 MM	1110
53 6 GCORE_CLIM	0.3 MM	0.20 MM	1111
53 6 GCORE_SS	0.3 MM	0.20 MM	1112
53 6 GCORE_ST	0.3 MM	0.20 MM	1113
53 6 GCORE_SW_R	0.6 MM	0.20 MM	1114

		MIN_LINE_WIDTH	MIN_NECK_WIDTH	
53	GCORE_CSCOMP	0.3 MM	0.20 MM	0.00
53	GCORE_CSF	0.3 MM	0.20 MM	0.00
53	GCORE_LLINE	0.3 MM	0.20 MM	0.00
53	GCORE_RT	0.3 MM	0.20 MM	0.00
53	GCORE_EN	0.3 MM	0.20 MM	0.00
53	GCORE_COMP	0.3 MM	0.20 MM	0.00
53	GCORE_FB	0.3 MM	0.20 MM	0.00
53	GCORE_FBRTN	0.3 MM	0.20 MM	0.00
53	GCORE_PMON	0.3 MM	0.20 MM	0.00
53	GCORE_PMONFS	0.3 MM	0.20 MM	0.00
53	GCORE_RPM	0.3 MM	0.20 MM	0.00
53	GCORE_VRPM	0.3 MM	0.20 MM	0.00
53	GCORE_FB_R	0.3 MM	0.20 MM	0.00

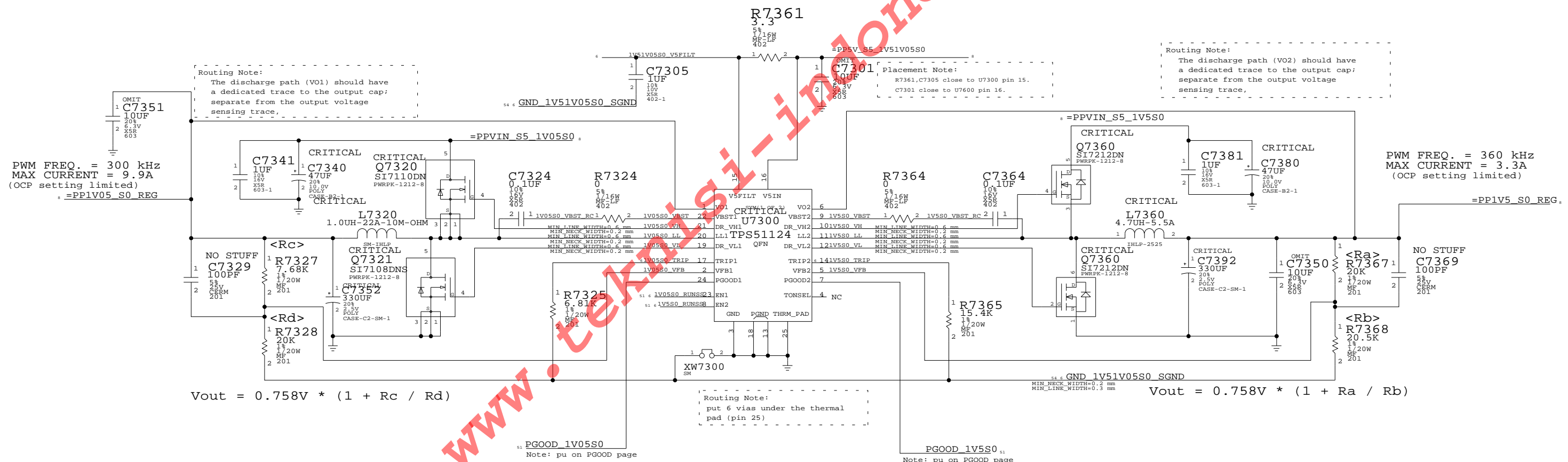
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SIZE D	DRAWING NUMBER 051-7230	REV. J
SCALE NONE	SHT 72	OF 109

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V

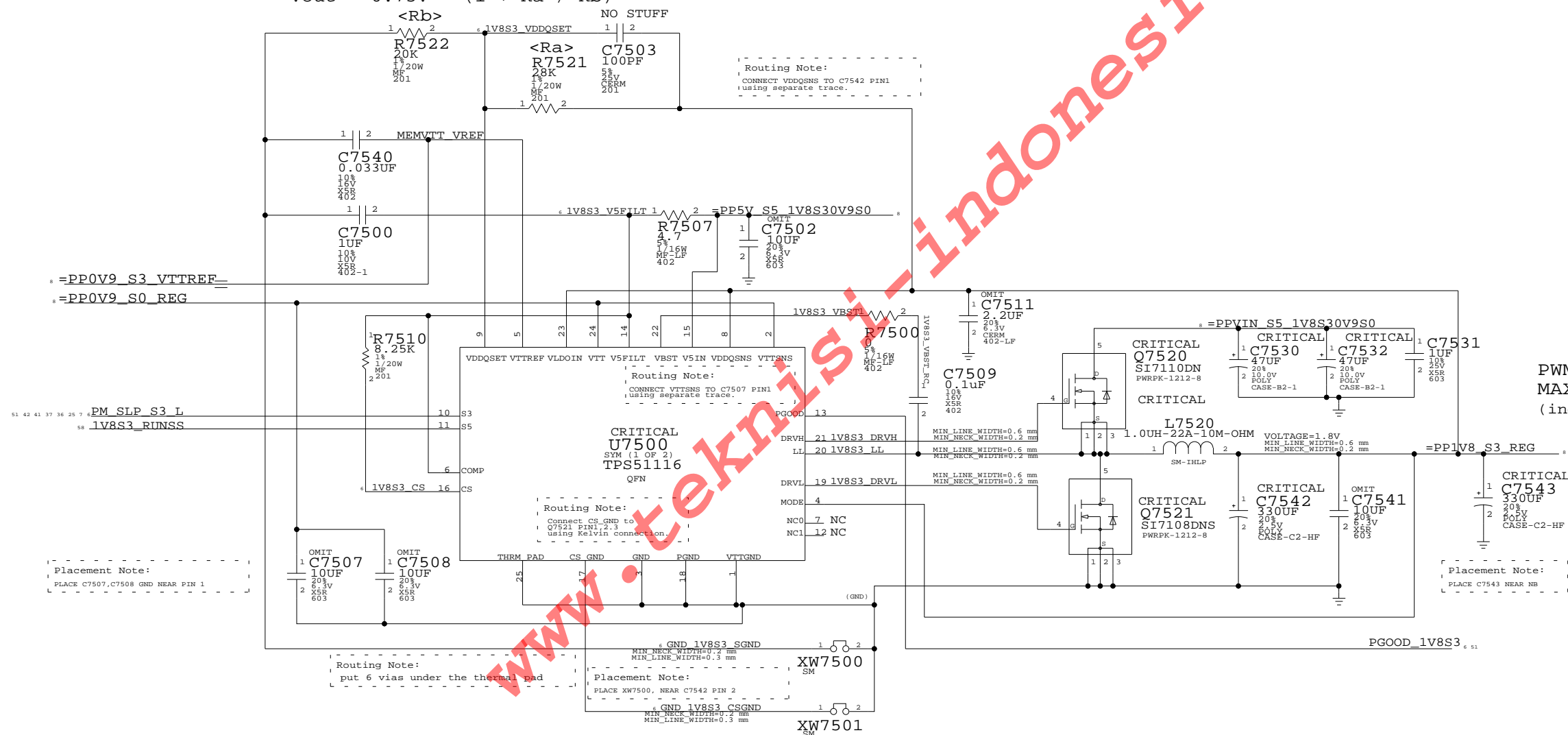


1.5V/1.05V Supplies
SYNC_MASTER=M70 SYNC_DATE=01/09/2007
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1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V

$$V_{out} = 0.75V * (1 + R_a / R_b)$$



PWM FREQ. = 400 kHz
MAX CURRENT = 11A
(inductor limited)

1.8V/0.9V Supplies

SYNC_MASTER=M70	SYNC_DATE=01/09/2007
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SIZE	DRAWING NUMBER	REV.
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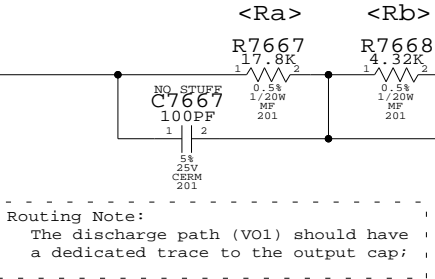
D	051-7230
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SCALE	SHT	OF
NONE	75	109

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

$$V_{out} = 1V * (1 + R_a / R_b)$$
$$5.120V = 1V * (1 + 17.8K / 4.32K)$$



Routing Note:
The discharge path (VO2) should have
a dedicated trace to the output cap;
separate from the output voltage
sensing trace,

PWM FREQ. = 280 kHz
MAX CURRENT = 6.0A
(inductor limited)
=PP5V_S5_REG

PWM FREQ. = 430 kHz
MAX CURRENT = 7.8A
(OCP setting limited)
=PP3V3_S5_REG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7680	KEMET TS20V336M016AT0457690
128S0093	128S0092	?	C7640	KEMET TS20V336M016AT0457690

Placement Note:
R7601,C7605 close to U7600 pin 20.
C7602 close to U7600 pin 22.
C7604 close to U7600 pin 21.
C7603 close to U7600 pin 19.
R7605,R7603 close to U7600.

5V/3.3V Supplies

SYNC_MASTER=M70

SYNC_DATE=02/01/2007

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APPLE INC.

SIZE D

DRAWING NUMBER 051-7230

REV. J

SCALE NONE

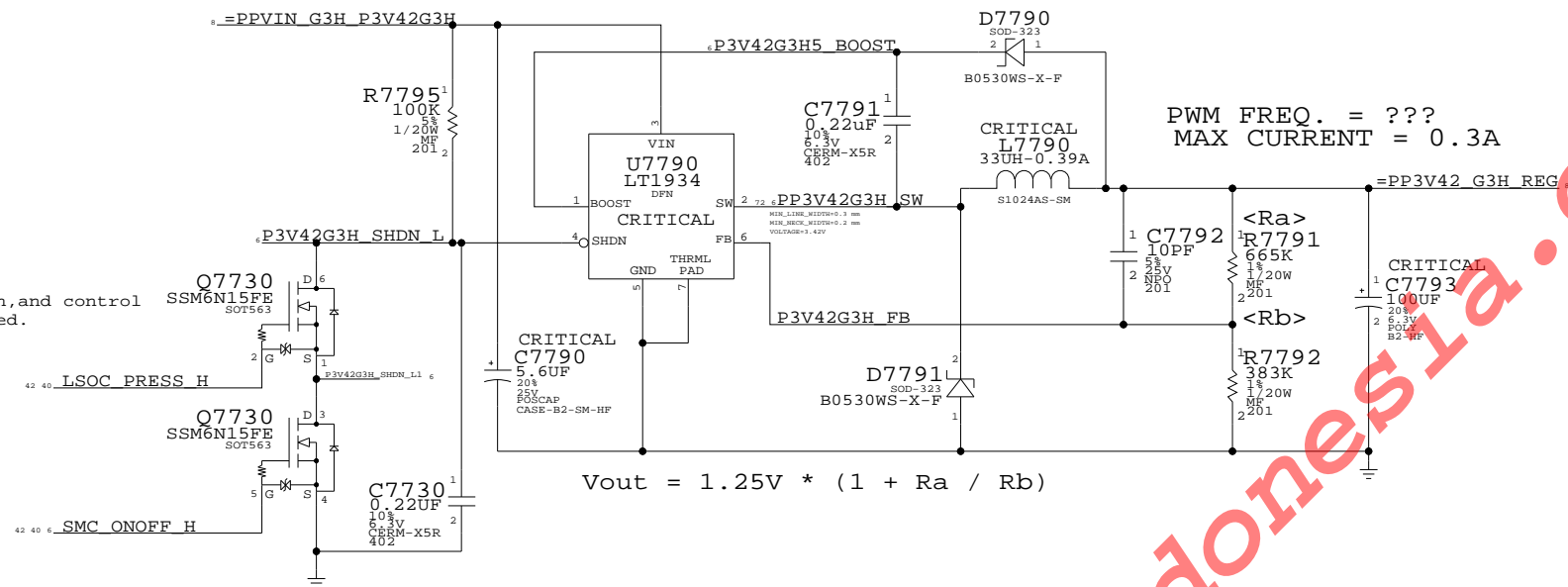
SHT 76

OF 109

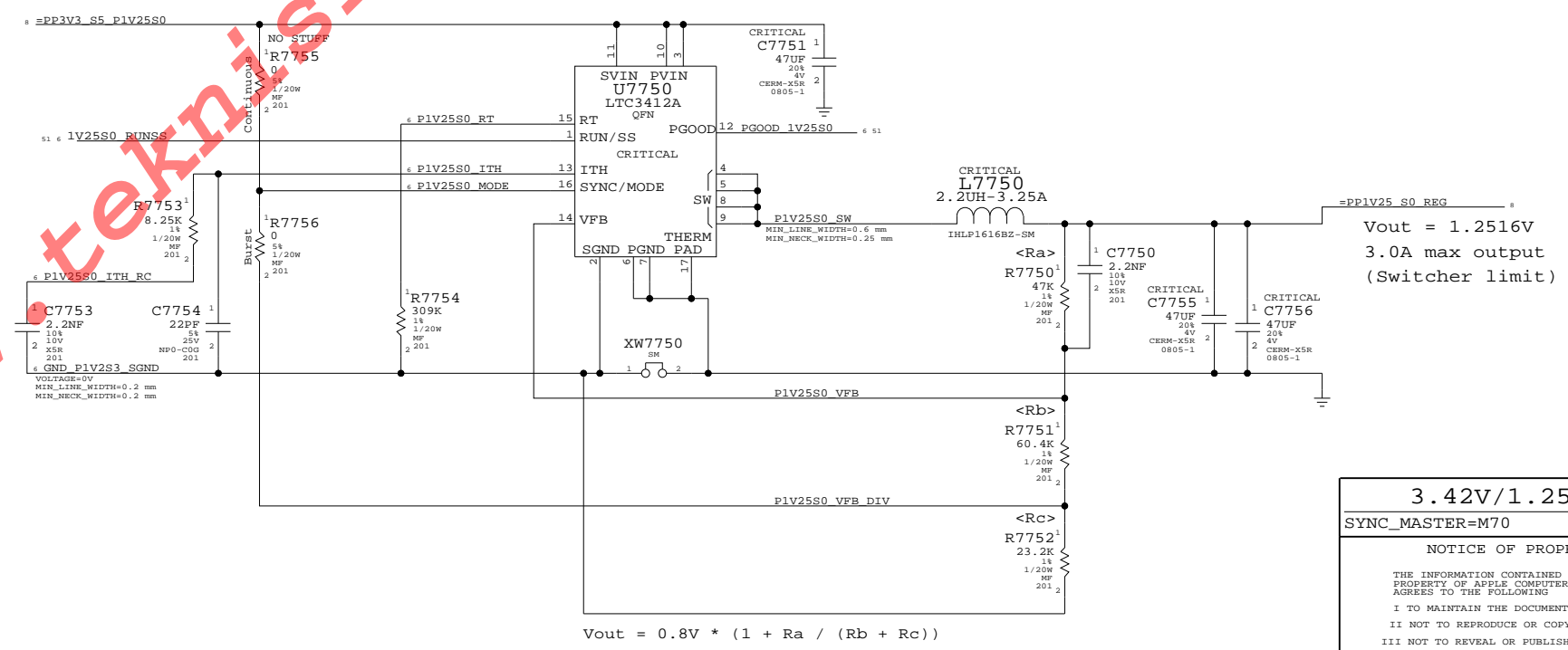
3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator

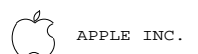
Q7730 will pull down
P3V42G3H_SHDN_L in the event
of a keyboard SMC Reset
generated when left shift,option,and control
and the power button is depressed.



1.25V S0 REGULATOR



3.42V/1.25V Switcher
SYNC_MASTER=M70 SYNC_DATE=01/09/2007
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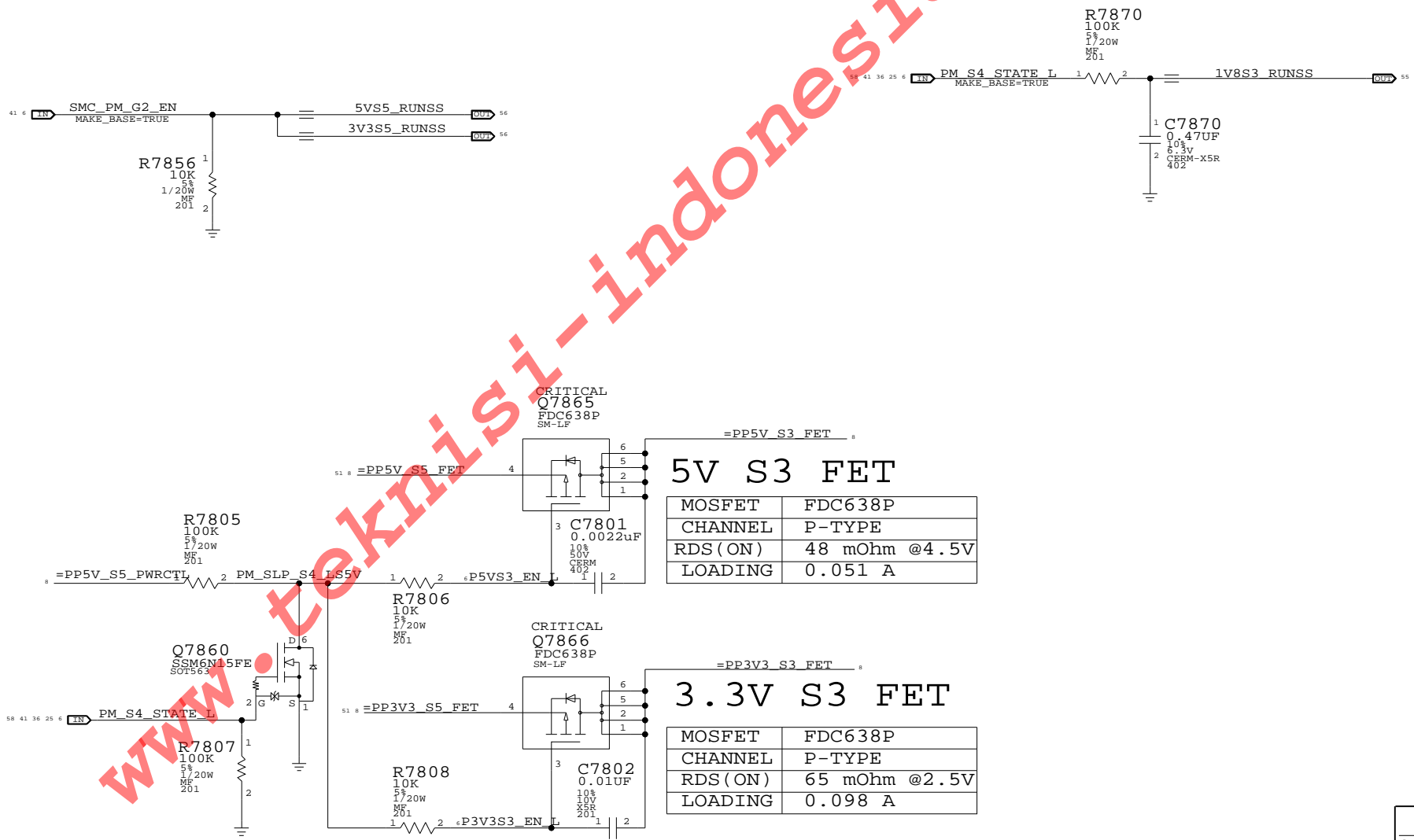
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT	OF
NONE	77	109

S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL

1.8V S3 RUN/SS CONTROL



5V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

S3 FET & S3/S5 Control
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

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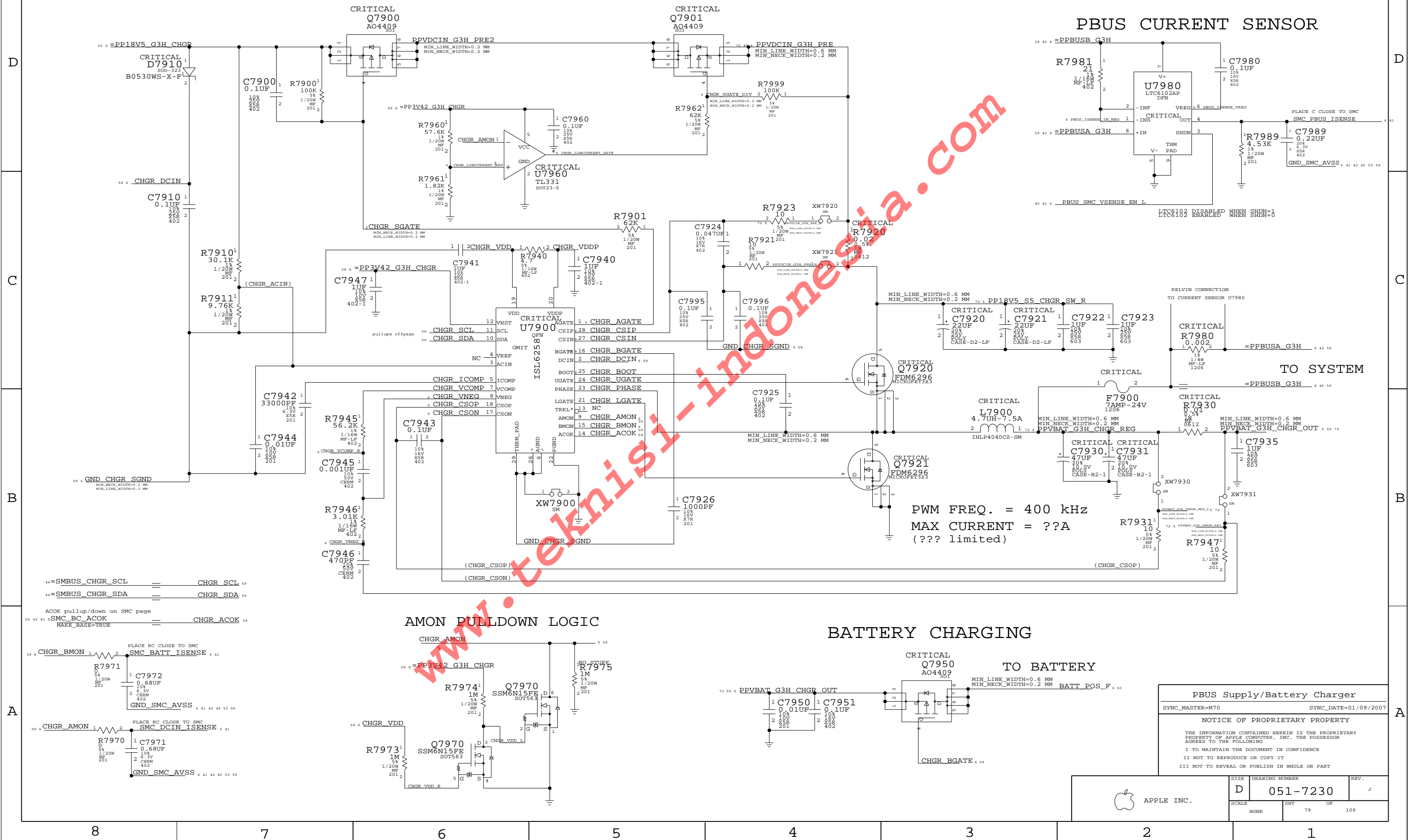
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

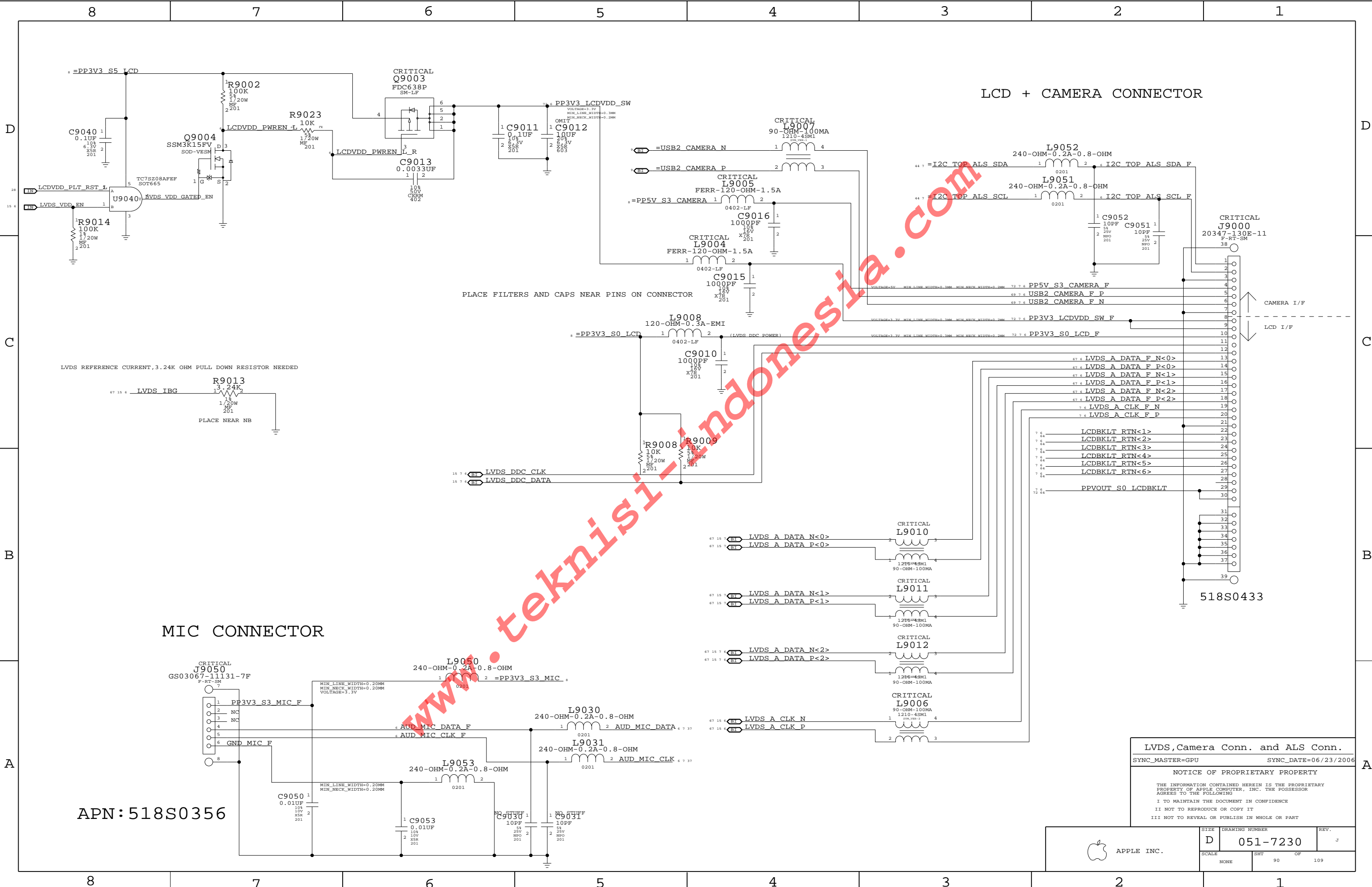
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
SCALE		SHT	OF
NONE		78	109

PBUS SUPPLY / BATTERY CHARGER





LCD + CAMERA CONNECTOR

MIC CONNECTOR

APN:518S0356

LVDS,Camera Conn. and ALS Conn.

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

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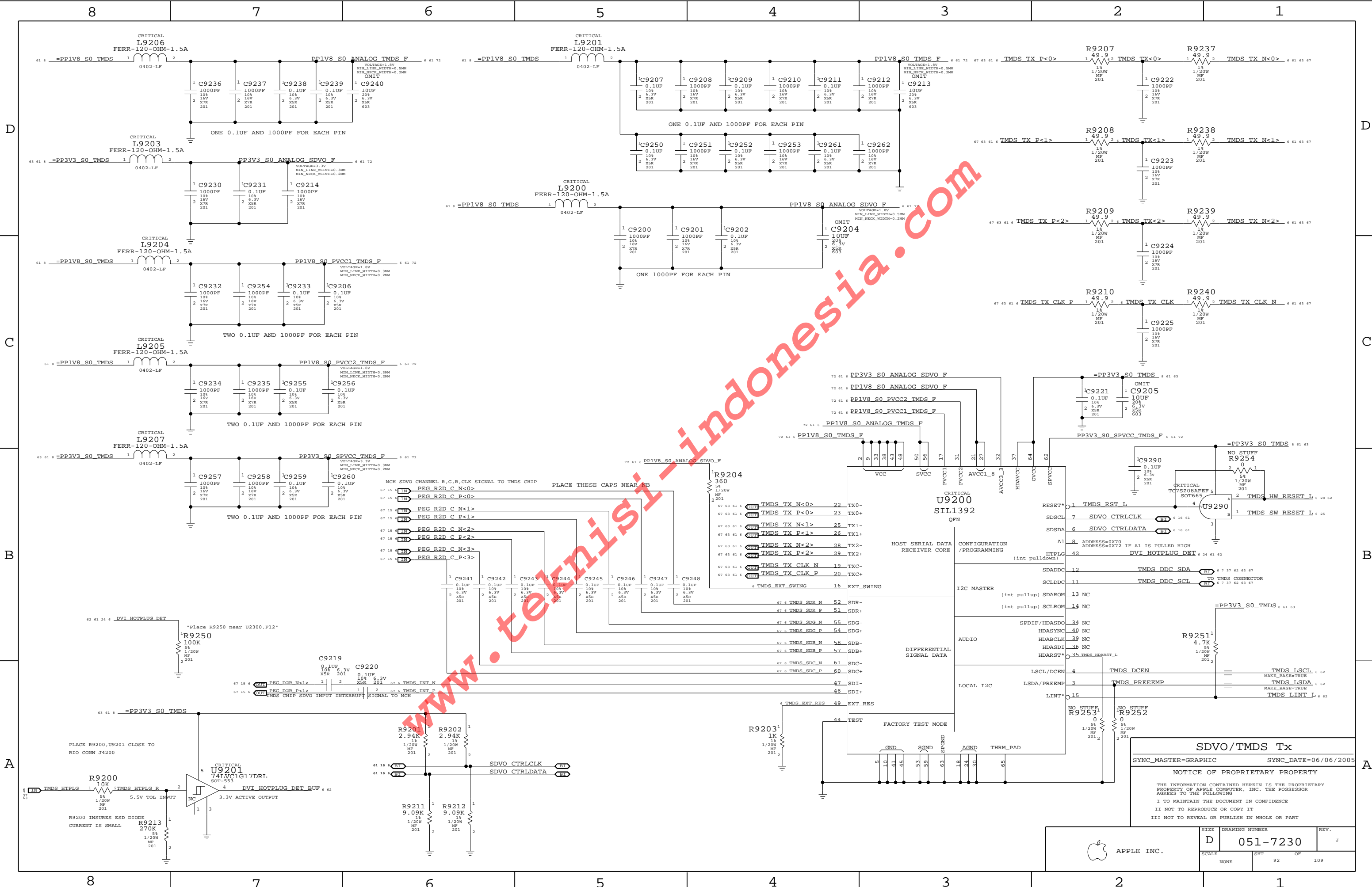


APPLE INC.

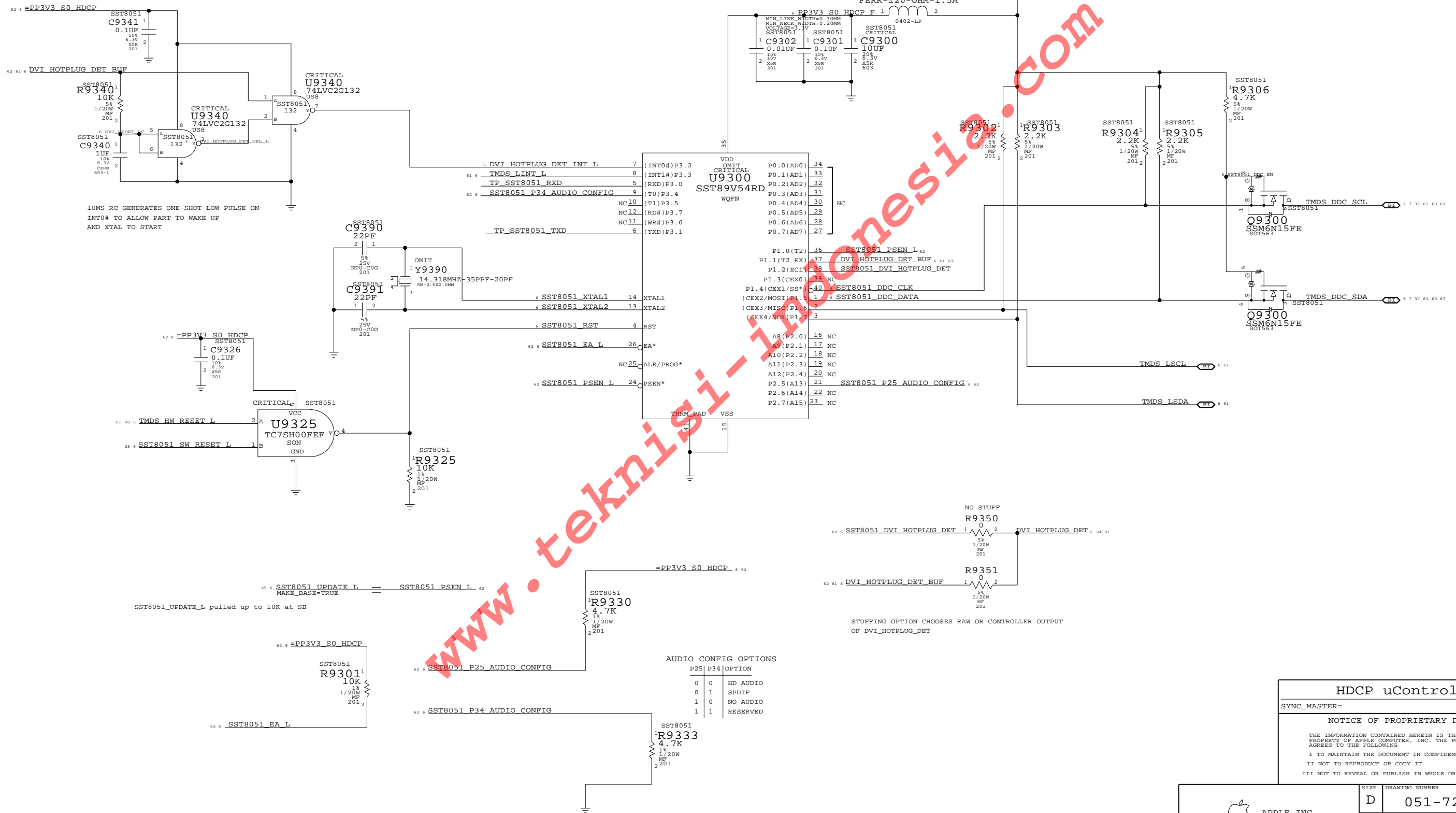
SIZE DRAWING NUMBER REV.

D 051-7230 J

SCALE NONE SHT 90 OF 109



PP3V3 S0 HDCP F 1 2
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
0402-LF



AUDIO CONFIG OPTIONS		
P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

```

HDCP uController
-----
SYNC_MASTER=                                SYNC_DATE=
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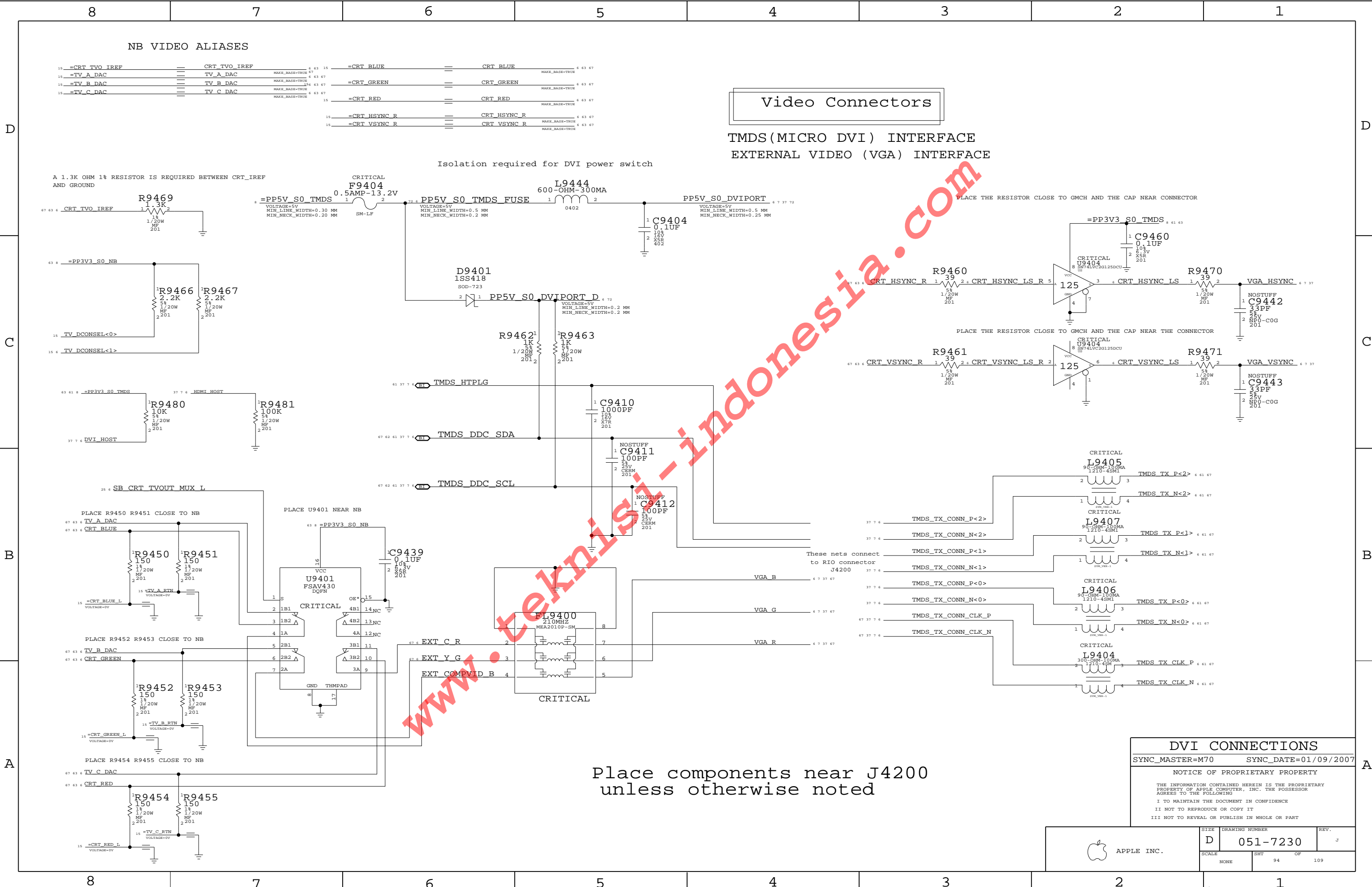
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NB VIDEO ALIASES

=CRT_TVO_IREF	CRT_TVO_IREF	MAKE_BASE=TRUE	6	63	67
=TV_A_DAC	TV_A_DAC	MAKE_BASE=TRUE	6	63	67
=TV_B_DAC	TV_B_DAC	MAKE_BASE=TRUE	6	63	67
=TV_C_DAC	TV_C_DAC	MAKE_BASE=TRUE	6	63	67
=CRT_BLUE	CRT_BLUE	MAKE_BASE=TRUE	6	63	67
=CRT_GREEN	CRT_GREEN	MAKE_BASE=TRUE	6	63	67
=CRT_RED	CRT_RED	MAKE_BASE=TRUE	6	63	67
=CRT_HSYNC_R	CRT_HSYNC_R	MAKE_BASE=TRUE	6	63	67
=CRT_VSYNC_R	CRT_VSYNC_R	MAKE_BASE=TRUE	6	63	67

Video Connectors

TMDS(MICRO DVI) INTERFACE
EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

These nets connect to RIO connector J4200

Place components near J4200 unless otherwise noted

DVI CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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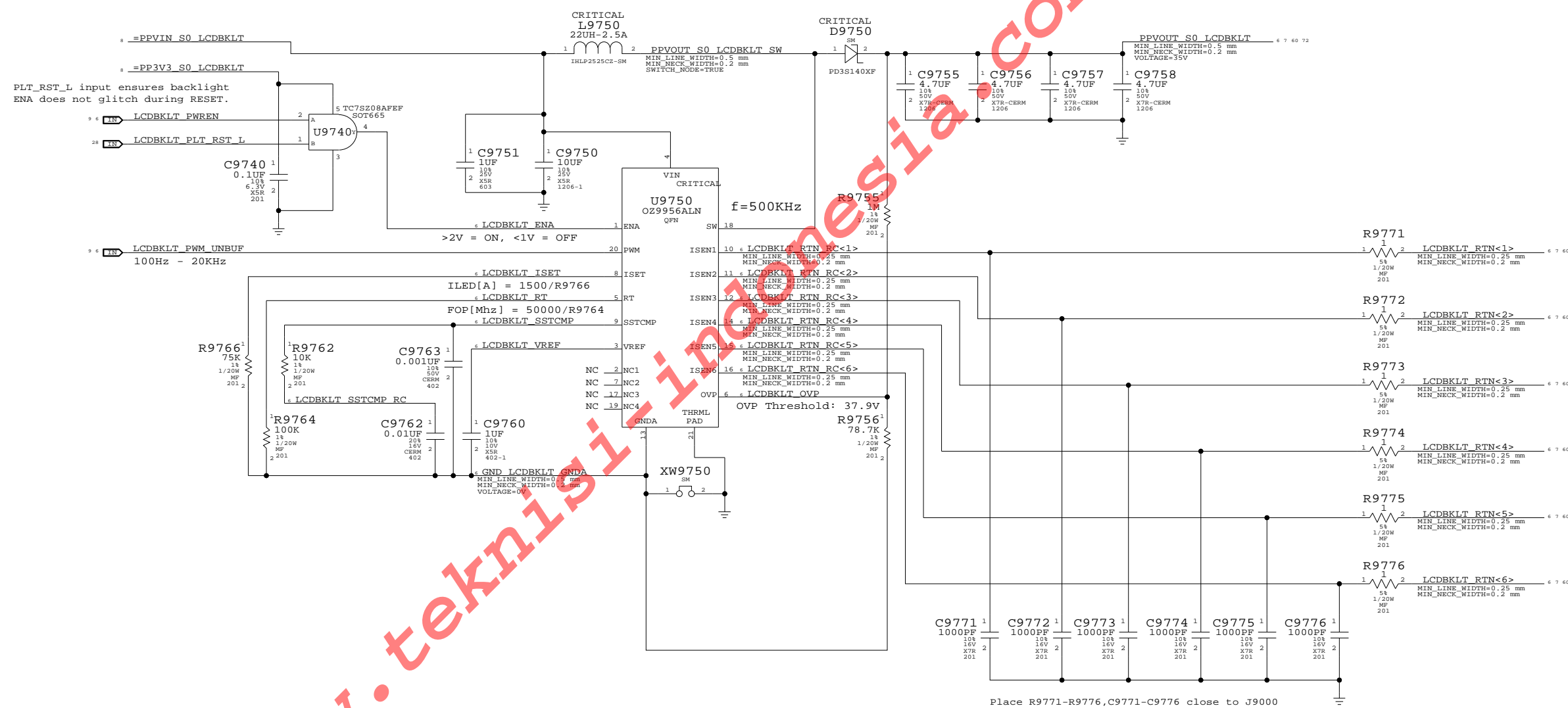
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	D	051-7230		J
SCALE		SHT	OF	109
NONE		94		

LED Backlight Driver



Place R9771-R9776,C9771-C9776 close to J9000

LED Backlight Driver

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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	D	051-7230		J
SCALE		SHT	OF	REV.
NONE		97	109	

Apple Inc.

8

7

6

5

4

3

2

1

8		7		6		5		4		3		2		1	
PCI-Express / DMI Bus Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP							
PCIE_100D		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
DMI_100D		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE_SPACING	WEIGHT											
PCIE		*	20 MIL	?											
PCIE_R2D_2_Pcie_R2D		*	0.228 MM	?											
PCIE_D2R_2_Pcie_D2R		*	0.228 MM	?											
PCIE_R2D_2_Pcie_D2R		*	0.300 MM	?											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
PCIE_R2D		PCIE_R2D	*	PCIE_R2D_2_Pcie_R2D											
PCIE_D2R		PCIE_D2R	*	PCIE_D2R_2_Pcie_D2R											
PCIE_R2D		PCIE_D2R	*	PCIE_R2D_2_Pcie_D2R											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
DMI_N2S		DMI_N2S	*	DMI_N2S_2_DMI_N2S											
DMI_S2N		DMI_S2N	*	DMI_S2N_2_DMI_S2N											
DMI_N2S		DMI_S2N	*	DMI_N2S_2_DMI_S2N											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
PCIE_R2D		PWR	*	BUS2PWR_GND											
PCIE_R2D		GND	*	BUS2PWR_GND											
PCIE_D2R		PWR	*	BUS2PWR_GND											
PCIE_D2R		GND	*	BUS2PWR_GND											
DMI_N2S		PWR	*	BUS2PWR_GND											
DMI_N2S		GND	*	BUS2PWR_GND											
DMI_S2N		PWR	*	BUS2PWR_GND											
DMI_S2N		GND	*	BUS2PWR_GND											
LVDS		PWR	*	BUS2PWR_GND											
LVDS		GND	*	BUS2PWR_GND											
TMDS		PWR	*	BUS2PWR_GND											
TMDS		GND	*	BUS2PWR_GND											
Video Signal Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP							
LVDS_100D		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
CRT_50S		*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
CRT_55S		*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
TMDS_100D		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE_SPACING	WEIGHT											
LVDS		*	20 MIL	?		DG Says 40 mil spacing minimum									
CRT		*	25 MIL	?											
CRT_2CRT		*	20 MIL	?											
CRT_SYNC		*	25 MIL	?		DG Says 30 mil spacing minimum									
CRT_SYNC2SYNC		*	20 MIL	?											
TVDAC		*	25 MIL	?		DG Says 40 mil spacing minimum									
TVDAC_2TVDAC		*	20 MIL	?											
LVDS2LVDS		*	0.300 MM	?											
TMDS		*	20 MIL	?											
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET											
CRT		CRT	*	CRT_2CRT											
CRT_SYNC		CRT_SYNC	*	CRT_SYNC2SYNC											
TVDAC		TVDAC	*	TVDAC_2TVDAC											
LVDS		LVDS	*	LVDS2LVDS											
LVDS signals are 100-ohm +/- 20% differential impedance. CRT & TVDAC signal single-ended impedance varies by location: - 37.5-ohm +/- 15% from GMCH to first termination resistor. - 50-ohm +/- 15% from first to second termination resistor. - 55-ohm +/- 15% from second termination resistor to connector. CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance. SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.															
Electrical Constraints															
ELECTRICAL_CONSTRAINT_SET		PHYSICAL		SPACING											
PEG_R2D		PCIE_100D		PCIE_R2D		PEG_R2D P<15..0>									
		PCIE_100D		PCIE_R2D		PEG_R2D N<15..0>									
		PCIE_100D		PCIE_R2D		PEG_R2D C P<15..0>									
		PCIE_100D		PCIE_R2D		PEG_R2D C N<15..0>									
PEG_D2R		PCIE_100D		PCIE_D2R		PEG_D2R P<15..0>									
		PCIE_100D		PCIE_D2R		PEG_D2R N<15..0>									
		PCIE_100D		PCIE_D2R		PEG_D2R C P<15..0>									
		PCIE_100D		PCIE_D2R		PEG_D2R C N<15..0>									
DMI_N2S		DMI_100D		DMI_N2S		DMI_N2S P<3..0>									
		DMI_100D		DMI_N2S		DMI_N2S N<3..0>									
DMI_S2N		DMI_100D		DMI_S2N		DMI_S2N P<3..0>									
		DMI_100D		DMI_S2N		DMI_S2N N<3..0>									
LVDS_A_CLK		LVDS_100D		LVDS		LVDS_A_CLK P									
LVDS_A_CLK		LVDS_100D		LVDS		LVDS_A_CLK N									
LVDS_A_DATA		LVDS_100D		LVDS		LVDS_A_DATA P<3..0>									
LVDS_A_DATA		LVDS_100D		LVDS		LVDS_A_DATA N<2..0>									
LVDS_A_DATA		LVDS_100D		LVDS		LVDS_A_DATA P P<2..0>									
LVDS_A_DATA		LVDS_100D		LVDS		LVDS_A_DATA N N<2..0>									
LVDS_A_DATA3		LVDS_100D		LVDS		LVDS_A_DATA P<3>									
LVDS_A_DATA3		LVDS_100D		LVDS		LVDS_A_DATA N<3>									
LVDS_B_CLK		LVDS_100D		LVDS		LVDS_B_CLK P									
LVDS_B_CLK		LVDS_100D		LVDS		LVDS_B_CLK N									
LVDS_B_DATA		LVDS_100D		LVDS		LVDS_B_DATA P<2..0>									
LVDS_B_DATA		LVDS_100D		LVDS		LVDS_B_DATA N<2..0>									
LVDS_B_DATA3		LVDS_100D		LVDS		LVDS_B_DATA P<3>									
LVDS_B_DATA3		LVDS_100D		LVDS		LVDS_B_DATA N<3>									
LVDS_IBG		LVDS_100D		LVDS		LVDS_IBG									
CRT_TVO_IREF		CRT_50S		CRT		CRT_TVO_IREF									
CRT_RED		CRT_50S		CRT		CRT_RED									
CRT_GREEN		CRT_50S		CRT		CRT_GREEN									
CRT_BLUE		CRT_50S		CRT		CRT_BLUE									
CRT_HSYNC		CRT_55S		CRT_SYNC		CRT_HSYNC_R									
CRT_VSYNC		CRT_55S		CRT_SYNC		CRT_VSYNC_R									
TV_A_DAC		CRT_50S		TVDAC		TV_A_DAC									
TV_B_DAC		CRT_50S		TVDAC		TV_B_DAC									
TV_C_DAC		CRT_50S		TVDAC		TV_C_DAC									
EXT_COMEVID_B		CRT_50S		CRT		EXT_COMEVID_B									
EXT_Y_G		CRT_50S		CRT		EXT_Y_G									
EXT_C_R		CRT_50S		CRT		EXT_C_R									
VGA_R		CRT_50S		CRT		VGA_R									
VGA_G		CRT_50S		CRT		VGA_G									
VGA_B		CRT_50S		CRT		VGA_B									
		PCIE_100D		PCIE_R2D		TMDS_SDB_P									
		PCIE_100D		PCIE_R2D		TMDS_SDB_N									
		PCIE_100D		PCIE_R2D		TMDS_SDC_P									
		PCIE_100D		PCIE_R2D		TMDS_SDC_N									
		PCIE_100D		PCIE_R2D		TMDS_SDG_P									
		PCIE_100D		PCIE_R2D		TMDS_SDG_N									
		PCIE_100D		PCIE_R2D		TMDS_SDR_P									
		PCIE_100D		PCIE_R2D		TMDS_SDR_N									
TMDS_100D		TMDS				TMDS_TX_CLK_P									
TMDS_100D		TMDS				TMDS_TX_CLK_N									
PCIE_100D		PCIE_D2R				TMDS_INT_P									
PCIE_100D		PCIE_D2R				TMDS_INT_N									
TMDS_100D		TMDS				TMDS_TX_CONN_CLK_P									
TMDS_100D		TMDS				TMDS_TX_CONN_CLK_N									
TMDS_100D		TMDS				TMDS_CONN_P<3..0>									
TMDS_100D		TMDS				TMDS_CONN_N<3..0>									
TMDS_100D		TMDS				TMDS_TX_P<3..0>									
TMDS_100D		TMDS				TMDS_TX_N<3..0>									
SMB_55S		SMB				TMDS_DPC_SCL									
SMB_55R		SMB				TMDS_DPC_SDA									
NB Constraints															
SYNC_MASTER=T9 SYNC_DATE=01/30/2007															
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APPLE INC. D 051-7230 J															
SCALE NONE SHT 101 OF 109															

8		7		6		5		4		3		2		1	
DDR2 Memory Bus Constraints															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
MEM_45S		*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD							
MEM_55S		ISL3, ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
MEM_55S		*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
MEM_87D		*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF							
MEM_85D		*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF							
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT		NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET					
MEM_CLK2MEM		*	=2.28:1_SPACING	?		MEM_CLK		GND	*	GND_P2MM					
MEM_CTRL2CTRL		*	=1:1_SPACING	?		MEM_CMD		GND	*	GND_P2MM					
MEM_CTRL2MEM		*	=2.28:1_SPACING	?		MEM_CTRL		GND	*	GND_P2MM					
MEM_CMD2CMD		*	=1:1_SPACING	?		MEM_DATA		GND	*	GND_P2MM					
MEM_CMD2MEM		*	=2.28:1_SPACING	?		MEM_DQS		GND	*	GND_P2MM					
MEM_DATA2DATA		*	=1:1_SPACING	?		MEM_CLK		PP1V8_MEM	*	PWR_P2MM					
MEM_DATA2MEM		*	=2.28:1_SPACING	?		MEM_CTRL		PP1V8_MEM	*	PWR_P2MM					
MEM_DQS2MEM		*	=2.28:1_SPACING	?		MEM_DATA		PP1V8_MEM	*	PWR_P2MM					
MEM_20THRR		*	25 MIL	?		MEM_DQS		PP1V8_MEM	*	PWR_P2MM					
MEM_CLK		*	*	MEM_20OTHER		NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET					
MEM_CTRL		*	*	MEM_20OTHER		MEM_CLK		NB_STATIC	*	PWR_P2MM					
MEM_CMD		*	*	MEM_20OTHER		MEM_CTRL		NB_STATIC	*	PWR_P2MM					
MEM_DATA		*	*	MEM_20OTHER		MEM_DATA		NB_STATIC	*	PWR_P2MM					
MEM_DQS		*	*	MEM_20OTHER		MEM_DQS		NB_STATIC	*	PWR_P2MM					
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET		MEM_CMD		NB_STATIC	*	PWR_P2MM					
MEM_CLK		MEM_CLK	*	MEM_CLK2MEM		NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET					
MEM_CLK		MEM_CTRL	*	MEM_CLK2MEM		MEM_DQS		MEM_CLK	*	MEM_DQS2MEM					
MEM_CLK		MEM_CMD	*	MEM_CLK2MEM		MEM_DQS		MEM_CTRL	*	MEM_DQS2MEM					
MEM_CLK		MEM_DATA	*	MEM_CLK2MEM		MEM_DQS		MEM_CMD	*	MEM_DQS2MEM					
MEM_CLK		MEM_DQS	*	MEM_CLK2MEM		MEM_DQS		MEM_DATA	*	MEM_DQS2MEM					
MEM_DQS		MEM_DQS	*	MEM_DQS2MEM		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
MEM_CMD		MEM_CLK	*	MEM_CMD2MEM		MEM_CMD		MEM_CLK	*	MEM_CMD2MEM					
MEM_CMD		MEM_CTRL	*	MEM_CMD2MEM		MEM_CMD		MEM_CTRL	*	MEM_CMD2MEM					
MEM_CMD		MEM_CMD	*	MEM_CMD2CMD		MEM_CMD		MEM_CMD	*	MEM_CMD2MEM					
MEM_CMD		MEM_DATA	*	MEM_CMD2MEM		MEM_CMD		MEM_DATA	*	MEM_CMD2MEM					
MEM_CMD		MEM_DQS	*	MEM_CMD2MEM		MEM_CMD		MEM_DQS	*	MEM_CMD2MEM					
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET		MEM_CTRL		GND	*	BUS2PWR_GND					
MEM_CTRL		MEM_CLK	*	MEM_CTRL2MEM		MEM_CMD		PWR	*	BUS2PWR_GND					
MEM_CTRL		MEM_CTRL	*	MEM_CTRL2CTRL		MEM_CMD		GND	*	BUS2PWR_GND					
MEM_CTRL		MEM_CMD	*	MEM_CTRL2MEM		MEM_DATA		PWR	*	BUS2PWR_GND					
MEM_CTRL		MEM_DATA	*	MEM_CTRL2MEM		MEM_DATA		GND	*	BUS2PWR_GND					
MEM_CTRL		MEM_DQS	*	MEM_CTRL2MEM		MEM_DQS		GND	*	BUS2PWR_GND					
NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET		MEM_DATA		MEM_CLK	*	MEM_DATA2MEM					
MEM_DATA		MEM_CTRL	*	MEM_DATA2MEM		MEM_DATA		MEM_CTRL	*	MEM_DATA2MEM					
MEM_DATA		MEM_CMD	*	MEM_DATA2MEM		MEM_DATA		MEM_CMD	*	MEM_DATA2MEM					
MEM_DATA		MEM_DATA	*	MEM_DATA2DATA		MEM_DATA		MEM_DATA	*	MEM_DATA2MEM					
MEM_DATA		MEM_DQS	*	MEM_DATA2MEM		MEM_DATA		MEM_DQS	*	MEM_DATA2MEM					
PP0V9_S3M MEM NBVREFB		NET_SPACING_TYPE=NB_STATIC		8 16 21		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
PP0V9_S3M MEM NBVREFA		NET_SPACING_TYPE=NB_STATIC		8 16 21		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF1		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF2		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF3		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF4		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF5		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF6		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
NB VCCSM LF7		NET_SPACING_TYPE=NB_STATIC		6 18		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
=PP1V8_S3M MEM NB		NET_SPACING_TYPE=PP1V8_MEM		8 16 18 21		MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
GND		NET_SPACING_TYPE=GND				MEM_DQS		MEM_DQS	*	MEM_DQS2MEM					
Memory Net Properties															
ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL		SPACING									
MEM_87D		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK	
MEM_87D		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK		MEM_CLK	
MEM_45S		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL	
MEM_45S		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL	
MEM_45S		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL		MEM_CTRL	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
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MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
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MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
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MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
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MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD		MEM_CMD	
MEM_A_CMD															

8		7		6		5		4		3		2		1																																		
D	Disk Interface Constraints														D																																	
	<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>IDE_55S</td><td>*</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>SATA_55S</td><td>*</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=55_OHM_SE</td><td>=STANDARD</td><td>=STANDARD</td></tr><tr><td>SATA_100D</td><td>*</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td></tr></table>								PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD	SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD	SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							D
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																								
	IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD																																								
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	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT																																												
	IDE	*	=1.8:1_SPACING	?																																												
	SATA	*	20 MIL	?																																												
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9																																																
HD Audio Interface Constraints																																																
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																									
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD																																									
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT																																													
HDA	*	=1.8:1_SPACING	?																																													
SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1																																																
USB 2.0 Interface Constraints																																																
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																									
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD																																									
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT																																													
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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET																																													
USB	PWR	*	BUS2PWR_GND																																													
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	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																								
	SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD																																								
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	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT																																												
	SMB	*	=3:1_SPACING	?																																												
	SPI	*	=1.8:1_SPACING	?																																												
	SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17																																															
SB Constraints (1 of 2)																																																
SYNC_MASTER=T9 SYNC_DATE=01/30/2007																																																
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B															B																																	
A															A																																	

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
IDE_PDS	IDE_55S	IDE	IDE_PDD<15..0>	6 23 38
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	6 23 38
IDE_PDCS1_L	IDE_55S	IDE	IDE_PDCS1_L	6 23 38
IDE_PDCS3_L	IDE_55S	IDE	IDE_PDCS3_L	6 23 38
IDE_PDIOW_L	IDE_55S	IDE	IDE_PDIOW_L	6 23 38
IDE_PDIOF_L	IDE_55S	IDE	IDE_PDIOF_L	6 23 38
IDE_PDDACK_L	IDE_55S	IDE	IDE_PDDACK_L	6 23 38
IDE_PDDREQ	IDE_55S	IDE	IDE_PDDREQ	6 23 38
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	6 23 38
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	6 23 38
ODD_RST_SVTOL_L	IDE_55S	IDE	ODD_RST_SVTOL_L	6 23 38
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	9 23
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_N	9 23
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_P	9 23
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_N	9 23
SATA_A_D2R	SATA_100D	GND	SATA_A_D2R_P	9
SATA_A_D2R	SATA_100D	GND	SATA_A_D2R_N	9
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_C_P	9
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_C_N	9
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	9 23
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_N	9 23
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_P	9 23
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_N	9 23
SATA_B_D2R	SATA_100D	GND	SATA_B_D2R_P	9
SATA_B_D2R	SATA_100D	GND	SATA_B_D2R_N	9
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_C_P	9
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_C_N	9
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	9 23
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_N	9 23
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_P	9 23
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_N	9 23
SATA_A_D2R	SATA_100D	GND	SATA_C_D2R_P	9
SATA_A_D2R	SATA_100D	GND	SATA_C_D2R_N	9
SATA_A_D2R	SATA_100D	SATA	SATA_C_D2R_C_P	9
SATA_A_D2R	SATA_100D	SATA	SATA_C_D2R_C_N	9
SATA_RBIAS	SATA_55S	SATA	SATA_RBIAS	6 9 23
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	6 9 23
HDA_BIT_CLK_R	HDA_55S	HDA	HDA_BIT_CLK_R	6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	6 7 9 23 37
HDA_SYNC_R	HDA_55S	HDA	HDA_SYNC_R	6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	6 9 23 37
HDA_RST_L_R	HDA_55S	HDA	HDA_RST_L_R	6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	6 9 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0_CODEC	6 9 23
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	6 9 23
HDA_SDOUT_R	HDA_55S	HDA	HDA_SDOUT_R	6 23
USB_EXTN_P	USB_90D	USB	USB_EXTN_P	9 24
USB_EXTN_N	USB_90D	USB	USB_EXTN_N	9 24
USB_EXTN_MUXED_P	USB_90D	USB	USB_EXTN_MUXED_P	9
USB_EXTN_MUXED_N	USB_90D	USB	USB_EXTN_MUXED_N	9
USB_MINI_P	USB_90D	USB	USB_MINI_P	9 24
USB_MINI_N	USB_90D	USB	USB_MINI_N	9 24
USB_EXTD_P	USB_90D	USB	USB_EXTD_P	9 24
USB_EXTD_N	USB_90D	USB	USB_EXTD_N	9 24
USB_CAMERA_P	USB_90D	USB	USB_CAMERA_P	9 24
USB_CAMERA_N	USB_90D	USB	USB_CAMERA_N	9 24
USB_BT_P	USB_90D	USB	USB_BT_P	9 24
USB_BT_N	USB_90D	USB	USB_BT_N	9 24
USB_TP2D_P	USB_90D	USB	USB_TP2D_P	9 24
USB_TP2D_N	USB_90D	USB	USB_TP2D_N	9 24
USB_IR_P	USB_90D	USB	USB_IR_P	6 9 24
USB_IR_N	USB_90D	USB	USB_IR_N	6 9 24
USB_EXTB_P	USB_90D	USB	USB_EXTB_P	9 24
USB_EXTB_N	USB_90D	USB	USB_EXTB_N	9 24
USB_EXCARD_P	USB_90D	USB	USB_EXCARD_P	9 24
USB_EXCARD_N	USB_90D	USB	USB_EXCARD_N	9 24
USB_EXTC_P	USB_90D	USB	USB_EXTC_P	9 24
USB_EXTC_N	USB_90D	USB	USB_EXTC_N	9 24
USB2_AIRPORT_P_F	USB_90D	USB	USB2_AIRPORT_P_F	6 36
USB2_AIRPORT_N_F	USB_90D	USB	USB2_AIRPORT_N_F	6 36
USB2_CAMERA_F_P	USB_90D	USB	USB2_CAMERA_F_P	6 7 60
USB2_CAMERA_F_N	USB_90D	USB	USB2_CAMERA_F_N	6 7 60
USB2_EXTN_F_P	USB_90D	USB	USB2_EXTN_F_P	6 7 37 39
USB2_EXTN_F_N	USB_90D	USB	USB2_EXTN_F_N	6 7 37 39
USB2_3G_F_P	USB_90D	USB	USB2_3G_F_P	6 7 37 39
USB2_3G_F_N	USB_90D	USB	USB2_3G_F_N	6 7 37 39
USB_RBIAS	USB_60S	USB	USB_RBIAS	6 24
SMB_CLK	SMB_55S	SMB	SMB_CLK	25 44
SMB_DATA	SMB_55S	SMB	SMB_DATA	25 44
SMB_ME_CLK	SMB_55S	SMB	SMB_ME_CLK	25 44
SMB_ME_DATA	SMB_55S	SMB	SMB_ME_DATA	25 44
SPI_SCLK_R	SPI_55S	SPI	SPI_SCLK_R	6 24 49
SPI_SCLK	SPI_55S	SPI	SPI_SCLK	6 24 49
SPI_A_SCLK_R	SPI_55S	SPI	SPI_A_SCLK_R	6 43 49
SPI_B_SCLK_R	SPI_55S	SPI	SPI_B_SCLK_R	6 43 49
SPI_SI_R	SPI_55S	SPI	SPI_SI_R	6 24 49
SPI_SI	SPI_55S	SPI	SPI_SI	6 24 49
SPI_A_SI_R	SPI_55S	SPI	SPI_A_SI_R	6 43 49
SPI_B_SI_R	SPI_55S	SPI	SPI_B_SI_R	6 43 49
SPI_SO	SPI_55S	SPI	SPI_SO	6 24 43 49
SPI_A_SO_R	SPI_55S	SPI	SPI_A_SO_R	6 49
SPI_B_SO	SPI_55S	SPI	SPI_B_SO	6 49
SPI_B_SO_R	SPI_55S	SPI	SPI_B_SO_R	6 49
SPI_CE_R_L<0>	SPI_55S	SPI	SPI_CE_R_L<0>	6 24 49
SPI_CE_R_L<0>	SPI_55S	SPI	SPI_CE_R_L<0>	6 43 49
SPI_CE_R_L<1>	SPI_55S	SPI	SPI_CE_R_L<1>	6 24 43
SPI_CE_R_L<1>	SPI_55S	SPI	SPI_CE_R_L<1>	6 24 43

SB Constraints (1 of 2)

SYNC_MASTER=T9

SYNC_DATE=01/30/2007

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55G	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1 _{min} SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	RACING
	PCI_AD	PCI_558	PCI	PCI_AD<18..0>	9 24
	PCI_AD19	PCI_558	PCI	PCI_AD<19>	9 24
	PCI_AD20	PCI_558	PCI	PCI_AD<20>	9 24
	PCI_AD	PCI_558	PCI	PCI_AD<31..21>	9 24
	PCI_AD	PCI_558	PCI	PCI_PAR	9 24
	PCI_C_BE_L	PCI_558	PCI	PCI_C_BE_L<3..0>	9 24
	PCI_CNT1	PCI_558	PCI	PCI_IRDY_L	6 24
	PCI_CNT1	PCI_558	PCI	PCI_DEVSEL_L	6 24
	PCI_CNT1	PCI_558	PCI	PCI_PERR_L	6 24
	PCI_LOCK_L	PCI_558	PCI	PCI_LOCK_L	6 24
	PCI_CNT1	PCI_558	PCI	PCI_SERR_L	6 24
	PCI_CNT1	PCI_558	PCI	PCI_STOP_L	6 24
	PCI_CNT1	PCI_558	PCI	PCI_TRDY_L	6 24
	PCI_CNT1	PCI_558	PCI	PCI_FRAME_L	6 24
	PCI_FW_REQ_L	PCI_558	PCI	PCI_FW_REQ_L	6 24
	PCI_FW_GNT_L	PCI_558	PCI	PCI_FW_GNT_L	6 24
	PCI_REQ1_L	PCI_558	PCI	PCI_REQ1_L	6 24
	PCI_CNT1_L	PCI_558	PCI	PCI_GNT1_L	6 24
	PCI_REQ2_L	PCI_558	PCI	PCI_REQ2_L	6 24
	PCI_GNT2_L	PCI_558	PCI	PCI_GNT2_L	6 24
	INT_PIRQA_L	PCI_558	PCI	INT_PIRQA_L	6 24
	INT_PIRQB_L	PCI_558	PCI	INT_PIRQB_L	6 24
	INT_PIRQC_L	PCI_558	PCI	INT_PIRQC_L	6 24
	INT_PIRQD_L	PCI_558	PCI	INT_PIRQD_L	6 24
	INT_PIRQE_L	PCI_558	PCI	INT_PIRQE_L	6 24
	INT_PIRQF_L	PCI_558	PCI	INT_PIRQF_L	6 24
	PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_P	
	PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_N	
	PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_P	
	PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_N	
	PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_P	
	PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_N	
	PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_P	
	PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_N	
				PCIE_EXCARD_R2D_C_P	
				PCIE_EXCARD_R2D_C_N	
				PCIE_EXCARD_D2R_P	
				PCIE_EXCARD_D2R_N	
				PCIE_FW_R2D_C_P	
				PCIE_FW_R2D_C_N	
				PCIE_FW_D2R_P	
				PCIE_FW_D2R_N	
	PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_MINI_R2D_C_P	24 36
	PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_MINI_R2D_C_N	24 36
	PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_MINI_D2R_P	24 36
	PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_MINI_D2R_N	24 36
				PCIE_ENET_R2D_C_P	
				PCIE_ENET_R2D_C_N	
				PCIE_ENET_D2R_P	
				PCIE_ENET_D2R_N	
	GLAN_COMP			GLAN_COMP	6 23
	ENET_KBIAS			NINEVEH_KBIAS_P	
	ENET_KBIAS			NINEVEH_KBIAS	
	(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_P	
	(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_N	
		GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_P	
		GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_N	
	ENET_LAN	LAN_558	ENET_LAN	LAN_RSTSYN	
	ENET_LAN	LAN_558	ENET_LAN	LAN_R2D<2..0>	
	ENET_LAN	LAN_558	ENET_LAN	LAN_D2R<2..0>	
	ENET_GLAN_CLK	LAN_558	ENET_CLK	ENET_GLAN_CLK_R	
	ENET_GLAN_CLK	LAN_558	ENET_CLK	ENET_GLAN_CLK	
	ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	
	ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_N<0>	
	ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	
	ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_N<1>	
	ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	
	ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_N<2>	
	ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	
	ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_N<3>	
	CLINK_NB	CLINK_558	CLINK	CLINK_NB_CLK	6 16
	CLINK_NB	CLINK_558	CLINK	CLINK_NB_DATA	6 16
	CLINK_NB_RESET_L	CLINK_558	CLINK	CLINK_NB_RESET_L	6 16
	CLINK_WLAN	CLINK_558	CLINK	CLINK_WLAN_CLK	
	CLINK_WLAN	CLINK_558	CLINK	CLINK_WLAN_DATA	
	CLINK_WLAN_RESET_L	CLINK_558	CLINK	CLINK_WLAN_RESET_L	
	NB_CLINK_VREF	CLINK_12M1L	CLINK_VREF	NB_CLINK_VREF	6 16
	SB_CLINK_VREF0	CLINK_12M1L	CLINK_VREF	SB_CLINK_VREF0	6 25
	SB_CLINK_VREF1	CLINK_12M1L	CLINK_VREF	SB_CLINK_VREF1	6 25

8	7	6	5	4	3	2	1
M82 Board-Specific Spacing & Physical Constraints							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, ISL12, ISL13, BOTTOM				NO_TYPE, BGA		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2, ISL4, ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10, ISL11, ISL13	Y	0.215 MM	0.215 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP, BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2, ISL4, ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10, ISL11, ISL13	Y	0.091 MM	0.091 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP, BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2, ISL4, ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10, ISL11, ISL13	Y	0.070 MM	0.070 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2, ISL4, ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10, ISL11, ISL13	Y	0.070 MM	0.070 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP, BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP, BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP, BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP, BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
DEFAULT	*	0.1 MM	?				
STANDARD	*	=DEFAULT	?				
BGA_P1MM	*	0.1 MM	?				
BGA_P2MM	*	0.2 MM	?				
BGA_P3MM	*	0.3 MM	?				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
1:1_SPACING	*	0.1 MM	?				
1.5:1_SPACING	*	0.15 MM	?				
1.8:1_SPACING	*	0.18 MM	?				
2:1_SPACING	*	0.2 MM	?				
2.28:1_SPACING	*	0.228 MM	?				
2.5:1_SPACING	*	0.25 MM	?				
3:1_SPACING	*	0.3 MM	?				
4:1_SPACING	*	0.4 MM	?				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
GND	*	=STANDARD	?				
PP1V8_MEM	*	=STANDARD	?				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
GND_P2MM	*	0.2 MM	1000				
PWR_P2MM	*	0.2 MM	1000				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
NB_STATIC	*	=STANDARD	?				
M82 Rule Definitions							
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